

HP 13255

HP-IB INTERFACE MODULE

Manual Part No. 13255-91128

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NOTE: This document is part of the 264XX DATA TERMINAL product series Technical Information Package (HP 13255).

## 1.0 INTRODUCTION.

The HP-IB Interface Module provides the means of communication between various HP-IB external devices and the Data Terminal as prescribed in IEEE Standard Document 488-1975. Refer also to the Operating and Service Manual (HP Part No. 02640-90042) for additional information.

## 2.0 OPERATING PARAMETERS.

A summary of operating parameters for the HP-IB Interface Module is contained in tables 1.0 through 6.7.

Table 1.0 Physical Parameters

Part number	Nomenclature	Size ( L x W x D ) +/-0.100 Inches	Weight (Pounds)
02640-60128	HP-IB Interface PCA	12.5 x 4.0 x 0.7	0.40
Number of Backplane Slots Required: 1			

Table 2.0 Reliability and Environmental Information

=====		
Environmental:	( X ) HP Class B	( ) Other:
Restrictions:	Type tested at product level	
=====		
Failure Rate: 1.934		(percent per 1000 hours)
=====		

Table 3.0 Power Supply and Clock Requirements - Measured  
(At +/-5% Unless Otherwise Specified)

+5 Volt Supply	+12 Volt Supply	-12 Volt Supply	-42 Volt Supply
@ 700 mA	@ 25 mA	@ mA	@ mA
		NOT APPLICABLE	NOT APPLICABLE
115 volts ac		220 volts ac	
@ A		@ A	
NOT APPLICABLE		NOT APPLICABLE	
Clock Frequency: 4.915 MHz			

Table 4.0 Switch Definitions

PCA Designation	Function
A11,A10,A9,A4	Module Address Selection (see section 3.0)
PL0 thru PL6	Respond to poll by pulling $\overline{BUSn}$ low corresponding to closed PLn. (One exclusive PL closed switch position per module)
ATN	Interrupt on $\overline{ATN}$ line (If closed, $\overline{ATN2}$ must be open)
ATN2	Interrupt on $\overline{ATN2}$ line (If closed, $\overline{ATN}$ must be open)
FC	Firmware Control Word - Function depends on firmware application
TA	Talk Always }
LA	Listen Always }
B4,B3,B2,B1,B0	Device Address Selection } HP-IB
SC	System Controller }
	Switch open = 1
	Switch closed = 0

Table 5.0 Connector Information

Connector and Pin No.	Signal Name	Signal Description
P1, Pin 1	+5V	+5 Volt Power Supply
-2	GND	Ground Common Return (Power and Signal)
-3	SYS CLK	4.915 MHz System Clock
-4		Not used
-5	ADDR0	Negative True, Address Bit 0
-6	ADDR1	Negative True, Address Bit 1
-7	ADDR2	Negative True, Address Bit 2
-8	ADDR3	Negative True, Address Bit 3
-9	ADDR4	Negative True, Address Bit 4
-10	ADDR5	Negative True, Address Bit 5
-11	ADDR6	Negative True, Address Bit 6
-12	ADDR7	Negative True, Address Bit 7
-13	ADDR8	Negative True, Address Bit 8
-14	ADDR9	Negative True, Address Bit 9
-15	ADDR10	Negative True, Address Bit 10
-16	ADDR11	Negative True, Address Bit 11
-17		Not Used
-18		Not Used
-19		Not Used
-20		Not Used
-21	I/O	Negative True, Input Output/Memory
-22	GND	Ground Common Return (Power and Signal)

Table 5.0 Connector Information (Cont'd.)

Connector and Pin No.	Signal Name	Signal Description
P1, Pin A	GND	Ground Common Return (Power and Signal)
-B	POLL	Negative True, Polled Interrupt Identification Request
-C	+12V	+12 Volt Power Supply
-D	PWR ON	System Power On
-E	BUS0	Negative True, Data Bus Bit 0
-F	BUS1	Negative True, Data Bus Bit 1
-H	BUS2	Negative True, Data Bus Bit 2
-J	BUS3	Negative True, Data Bus Bit 3
-K	BUS4	Negative True, Data Bus Bit 4
-L	BUS5	Negative True, Data Bus Bit 5
-M	BUS6	Negative True, Data Bus Bit 6
-N	BUS7	Negative True, Data Bus Bit 7
-P	WRITE	Negative True, Write/Read Type Cycle
-R	ATN2	Negative True, CTU and Polled Interrupt Request
-S		Not Used
-T	PRIOR IN	Bus Controller Priority In
-U	PRIOR OUT	Bus Controller Priority Out
-V		Not Used
-W		Not Used
-X		Not Used
-Y	REQ	Negative True, Request (Bus Data Currently Valid)
-Z	ATN	Negative True, Data Comm Interrupt Request

Table 5.1 Connector Information

Connector and Pin No.	Signal Name	Signal Description
P2, Pin 1 through		
-6	GND	Ground Common Return for ATN,SRQ,IFC,NDAC, NRFD,DAV
-7	REN	Negative True, Remote Enable
-8	DI04	Negative True, Data Input/Output Bit 4
-9	DI03	Negative True, Data Input/Output Bit 3
-10	DI02	Negative True, Data Input/Output Bit 2
-11	DI01	Negative True, Data Input/Output Bit 1
-12		Not Used
-13	+5V	+5 volts
-14		Not Used
-15	GND	Ground Common Return (Logic)
-A	ATN	Negative True, Attention
-B	SRQ	Negative True, Service Request
-C	IFC	Negative True, Interface Clear
-D	NDAC	Negative True, Not Data Accepted
-E	NRFD	Negative True, Not Ready For Data
-F	DAV	Negative True, Data Valid
-H	EOI	Negative True, End Or Identify
-J	DI08	Negative True, Data Input/Output Bit 8
-K	DI07	Negative True, Data Input/output Bit 7
-L	DI06	Negative True, Data Input/Output Bit 6
-M	DI05	Negative True, Data Input/Output bit 5
Pin -N through		
-S		Not Used

Table 6.0 Module Bus Pin Assignments

Function	Value	Bus Signal
Performed: Read Interface Status	X	ADDR 15
	X	ADDR 14
Poll Bit: BUS0 through BUS6	X	ADDR 13
Depends on the setting of	X	ADDR 12
Switches PL0 through F06, respectively	A11	ADDR 11
	A10	ADDR 10
Module Address: (ADDR11,10,9,4)	A9	ADDR 9
Depends on the setting of	X	ADDR 8
Switches A4,A11,A10,A9	X	ADDR 7
	1	ADDR 6
Function Specifier: ADDR 6 = 1	X	ADDR 5
ADDR 1 = 0	A4	ADDR 4
ADDR 0 = 0	X	ADDR 3
	X	ADDR 2
	0	ADDR 1
Data Bus Bit Interpretation:	0	ADDR 0
B7 - X	B7	BUS 7
	B6	BUS 6
B6 - DMAACT	B5	BUS 5
0 = DMA inactive	B4	BUS 4
1 = DMA active	B3	BUS 3
	B2	BUS 2
B5 - BUFFUL	B1	BUS 1
0 = RAM buffer not full	B0	BUS 0
1 = RAM buffer full		
B4 - EOI		
0 = EOI (End Or Identify) not received		
1 = EOI received		
B3 - LSTBYT		
0 = Last data byte (Type 1) not received		
1 = Last data byte (Type 1) received		
B2 - SECADR		
0 = Secondary address not received		
1 = Secondary address received		
B1 - D0, Bit 9 from PHI (Most Significant)		
B0 - D1, Bit 8 from PHI		



Table 6.1 Module Bus Pin Assignments

Function Performed: Read Buffer Address (Interface RAM Buffer)	Value	Bus Signal
	X	ADDR 15
	X	ADDR 14
Poll Bit: BUS0 through BUS6	X	ADDR 13
Depends on the setting of	X	ADDR 12
Switches PL0 through PL6, respectively	A11	ADDR 11
	A10	ADDR 10
Module Address: (ADDR11,10,9,4)	A9	ADDR 9
Depends on the setting of	X	ADDR 8
Switches A4,A11,A10,A9	X	ADDR 7
	1	ADDR 6
Function Specifier: ADDR 6 = 1	X	ADDR 5
ADDR 1 = 0	A4	ADDR 4
ADDR 0 = 1	X	ADDR 3
	X	ADDR 2
	0	ADDR 1
Data Bus Bit Interpretation:	1	ADDR 0
B7 - A7, Buffer address bit 7	B7	BUS 7
B6 - A6, Buffer address bit 6	B6	BUS 6
B5 - A5, Buffer address bit 5	B5	BUS 5
B4 - A4, Buffer address bit 4	B4	BUS 4
B3 - A3, Buffer address bit 3	B3	BUS 3
B2 - A2, Buffer address bit 2	B2	BUS 2
B1 - A1, Buffer address bit 1	B1	BUS 1
B0 - A0, Buffer address bit 0	B0	BUS 0
	1=Logical 1=Bus Low 0=Logical 0=Bus High X=Don't Care	

Table 6.2 module bus Pin Assignments

Function	Value	Bus Signal
Performed: Read Jumpers (S2-8, S3-1 thru S3-7)	X	ADDR 15
	X	ADDR 14
Poll Bit: BUS0 through BUS6	X	ADDR 13
Depends on the setting of	X	ADDR 12
Switches PL0 through PL6, respectively	A11	ADDR 11
	A10	ADDR 10
Module Address: (ADDR11,10,9,4)	A9	ADDR 9
Depends on the setting of	X	ADDR 8
Switches A4,A11,A10,A9	X	ADDR 7
	1	ADDR 6
Function Specifier: ADDR 6 = 1	X	ADDR 5
ADDR 1 = 1	A4	ADDR 4
ADDR 0 = 0	X	ADDR 3
	X	ADDR 2
	1	ADDR 1
	0	ADDR 0
Data Bus Bit Interpretation:		
B7 - FC, Firmware Control word	B7	BUS 7
	B6	BUS 6
B6 - TA, } Talk Always	B5	BUS 5
PHI chip }	B4	BUS 4
B5 - LA, } Listen Always	B3	BUS 3
	B2	BUS 2
B4 - B4, HP-IB device address bit 4 }	B1	BUS 1
B3 - B3, HP-IB device address bit 3 }	B0	BUS 0
B2 - B2, HP-IB device address bit 2 }		
B1 - B1, HP-IB device address bit 1 }		
B0 - B0, HP-IB device address bit 0 }		

Address  
to which  
the PHI  
chip  
will  
respond when  
non-controller

11=Logical 1=Bus Low  
10=Logical 0=Bus High  
X=Don't Care

Table 6.3 Module Bus Pin Assignments

Function	Value	Bus Signal
Performed: Send Interface Command	X	ADDR 15
	X	ADDR 14
Poll Bit: BUS0 through BUS6	X	ADDR 13
Depends on the setting of	X	ADDR 12
Switches PL0 through PL6, respectively	A11	ADDR 11
	A10	ADDR 10
Module Address: (ADDR11,10,9,4)	A9	ADDR 9
Depends on the setting of	X	ADDR 8
Switches A4,A11,A10,A9	X	ADDR 7
	1	ADDR 6
Function Specifier: ADDR 6 = 1	X	ADDR 5
ADDR 1 = 0	A4	ADDR 4
ADDR 0 = 0	X	ADDR 3
	X	ADDR 2
	0	ADDR 1
Data Bus Bit Interpretation:	0	ADDR 0
B7 - X	B7	BUS 7
	B6	BUS 6
B6 - =1, RSTDMA, Reset DMA	B5	BUS 5
	B4	BUS 4
B5 - =1, INTENB, Interrupt enable	B3	BUS 3
	B2	BUS 2
B4 - =1, RSTBUF, Reset buffer address counters	B1	BUS 1
	B0	BUS 0
B3 - =1, PHI2BUF, Transfer data from PHI to buffer	=====	
B2 - =1, BUF2PHI, Transfer data from buffer to PHI	1=Logical 1=Bus Low	
	0=Logical 0=Bus High	
B1 - =1, ATNENB, ATN (HP-IB) to PHI enable	1X=Don't Care	
	=====	
B0 - =1, SRST, Soft reset		

Table 6.4 Module Bus Pin Assignments

Function	Value	Bus Signal
Performed: Read From PHI (LSI chip)	X	ADDR 15
	X	ADDR 14
Poll Bit: BUS0 through BUS6	X	ADDR 13
Depends on the setting of	X	ADDR 12
Switches PL0 through PL6, respectively	A11	ADDR 11
	A10	ADDR 10
Module Address: (ADDR11,10,9,4)	A9	ADDR 9
Depends on the setting of	X	ADDR 8
Switches A4,A11,A10,A9	X	ADDR 7
	0	ADDR 6
PHI Registers Selection: ADDR2,1,0 (ADDR2 MSB)	0	ADDR 5
Depends on which one of	A4	ADDR 4
eight registers (0 thru 7)	X	ADDR 3
is to be read	A2	ADDR 2
	A1	ADDR 1
Function Specifier: ADDR6 = 0	A0	ADDR 0
ADDR5 = 0		
	B7	BUS 7
	B6	BUS 6
Data Bus Bit Interpretation:	B5	BUS 5
	B4	BUS 4
B7 - D8, Data bit 7	B3	BUS 3
	B2	BUS 2
B6 - D9, Data bit 6	B1	BUS 1
	B0	BUS 0
B5 - D10, Data bit 5		
B4 - D11, Data bit 4		
B3 - D12, Data bit 3		
B2 - D13, Data bit 2		
B1 - D14, Data bit 1		
B0 - D15, Data bit 0		

1=Logical 1=Bus Low  
0=Logical 0=Bus High  
X=Don't Care

Table 6.5 Module Bus Pin Assignments

Function	Value	Bus Signal
Performed: Read From Buffer (Interface RAM Buffer)	X	ADDR 15
	X	ADDR 14
Poll Bit: BUS0 through BUS6	X	ADDR 13
Depends on the setting of	X	ADDR 12
Switches PL0 through PL6, respectively	A11	ADDR 11
	A10	ADDR 10
Module Address: (ADDR11,10,9,4)	A9	ADDR 9
Depends on the setting of	X	ADDR 8
Switches A4,A11,A10,A9	X	ADDR 7
	0	ADDR 6
Function Specifier: ADDR6 = 0	1	ADDR 5
ADDR5 = 1	A4	ADDR 4
	X	ADDR 3
	X	ADDR 2
	X	ADDR 1
	X	ADDR 0
	B7	BUS 7
	B6	BUS 6
	B5	BUS 5
	B4	BUS 4
	B3	BUS 3
	B2	BUS 2
	B1	BUS 1
	B0	BUS 0
Data Bus Bit Interpretation:	1=Logical 1=Bus Low	
B7 - D8, Data bit 7	0=Logical 0=Bus High	
B6 - D9, Data bit 6	1X=Don't Care	
B5 - D10, Data bit 5		
B4 - D11, Data bit 4		
B3 - D12, Data bit 3		
B2 - D13, Data bit 2		
B1 - D14, Data bit 1		
B0 - D15, Data bit 0		

Table 6.6 Module Bus Pin Assignments

Function	Value	Bus Signal
Performed: Write to PHI (LSI Chip)	X	ADDR 15
	X	ADDR 14
Poll Bit: BUS0 through BUS6	X	ADDR 13
Depends on the setting of	X	ADDR 12
Switches PL0 through PL6, respectively	A11	ADDR 11
	A10	ADDR 10
Module Address: (ADDR11,10,9,4)	A9	ADDR 9
Depends on the setting of	A8	ADDR 8
Switches A4,A11,A10,A9	X	ADDR 7
	0	ADDR 6
PHI registers Selection: ADDR2,1,0 (ADDR2 MSB)	0	ADDR 5
Depends on which one of	A4	ADDR 4
eight registers (1 thru 7)	A3	ADDR 3
is to be written to	A2	ADDR 2
	A1	ADDR 1
Function Specifier: ADDR6 = 0	A0	ADDR 0
ADDR5 = 0		
	B7	BUS 7
	B6	BUS 6
Address Bus Bit Interpretation:	B5	BUS 5
	B4	BUS 4
A8 - D0, Data bit 9	B3	BUS 3
	B2	BUS 2
A3 - D1, Data bit 8	B1	BUS 1
	B0	BUS 0
Data Bus Bit Interpretation:		
B7 - D8, Data bit 7		1=Logical 1=Bus Low
		0=Logical 0=Bus High
B6 - D9, Data bit 6		1X=Don't Care
B5 - D10, Data bit 5		
B4 - D11, Data bit 4		
B3 - D12, Data bit 3		
B2 - D13, Data bit 2		
B1 - D14, Data bit 1		
B0 - D15, Data bit 0		

Table 6.7 Module Bus Pin Assignments

Function	Value	Bus Signal
Performed: Write to Buffer (Interface RAM Buffer)	X	ADDR 15
	X	ADDR 14
Poll Bit: BUS0 through BUS6	X	ADDR 13
Depends on the setting of	X	ADDR 12
Switches PL0 through PL6, respectively	A11	ADDR 11
	A10	ADDR 10
Module Address: (ADDR11,10,9,4)	A9	ADDR 9
Depends on the setting of	A8	ADDR 8
Switches A4,A11,A10,A9	A7	ADDR 7
	0	ADDR 6
Function Specifier: ADDR6 = 0	1	ADDR 5
ADDR5 = 1	A4	ADDR 4
	A3	ADDR 3
Address Bus Bit Interpretation:	X	ADDR 2
	X	ADDR 1
A7 - =1, ENDBIT, Last byte to buffer	X	ADDR 0
	B7	BUS 7
A8 - D0, Data bit 9	B6	BUS 6
	B5	BUS 5
A3 - D1, Data bit 8	B4	BUS 4
Data Bus Bit Interpretation:	B3	BUS 3
	B2	BUS 2
B7 - D8, Data bit 7	B1	BUS 1
	B0	BUS 0
B6 - D9, Data bit 6		
B5 - D10, Data bit 5		
B4 - D11, Data bit 4		
B3 - D12, Data bit 3		
B2 - D13, Data bit 2		
B1 - D14, Data bit 1		
B0 - D15, Data bit 0		

1=Logical 1=Bus Low  
0=Logical 0=Bus High  
X=Don't Care

3.0 FUNCTIONAL DESCRIPTION. Refer to the block diagram, (figure 1), schematic diagram (figure 2), component location diagram (figure 3), and parts list 02640-60128 located in the appendix.

The purpose of the HP-IB Interface Module is to implement the intent of IEEE Standard 488-1975.

The HP-IB Interface Module consists of a bus instruction decoder, bus receivers, bus drivers, buffer address generator, buffer, DMA, EOI decoder, PHI register address multiplexer, status register, HP-IB address, interrupt logic, and HP-IB logical and electrical interfacing circuits.

### 3.1 BUS INSTRUCTION DECODER.

3.1.1 The bus instruction decoder consists of (U24), an LS136 Quad exclusive-OR (U43), an LS138 3-to-8 line decoder (U33), an LS139 2-to-4 line decoder, and several gates. This circuit uses control, bus, and address lines on the terminal busses to generate control signals on the PCA.

3.1.2 The LS136 (U24) Quad Exclusive-OR is the module address decoder. The module address is set by the four switches marked A4, A11, A10, and A9. When ADDR4, 11, 10, 9 match the number set by the switches, the module is selected and one of the enabling inputs (G1) of the LS138 (U43) 3/8 line decoder is enabled. The other two enabling inputs (G2A,B) are enabled by REO and I/O and ADDR6.

The LS139 (U33) 2/4 line decoder is enabled by the output of the Module Address Decoder and  $\overline{RE0}$  and  $\overline{I/O}$  and  $\overline{ADDR6}$ .  $\overline{ADDR6}$  determines which of the two line decoders is active.

WRITE, ADDR1, and ADDR0 connected to the LS138 (U43) are decoded and provide four strobes. WRITE, and ADDR5 connected to the LS139 produce four more.

ADDR6	WRITE	ADDR5	ADDR1	ADDR0	FUNCTION		
1	0	X	0	0	Read	I/F	Status
1	0	X	0	1	Read	Buffer	Address
1	0	X	1	0	Read		Jumpers
1	1	X	0	0	Send	I/F	Command
0	0	0	X	X	Read	from	PHI
0	0	1	X	X	Read	from	Buffer
0	1	0	X	X	Write	to	PHI
0	1	1	X	X	Write	to	Buffer

X= Don't care



- 3.1.4 In addition, the Send I/F Command strobe is "ANDed" with data bus lines to provide the following command strobes:

Data Bit 0= 1, Soft Reset (SRST)  
Data Bit 1= 1, ATN (HP-IB) to PHI Enable (ATNENB)  
Data Bit 2= 1, DMA to PHI (BUF2PHI)  
Data Bit 3= 1, PHI to DMA (PHI2BUF)  
Data Bit 4= 1, Reset Buffer Address (RSTBUF)  
Data Bit 5= 1, Interrupt Enable (INTENB)  
Data Bit 6= 1, Reset DMA (RSTDMA)

### 3.2 BUS RECEIVERS.

- 3.2.1 A three-state octal buffer driver LS240 (U37) is used to transfer the data from the terminal data bus to both the PHI chip and the RAM buffer. It is selected by strobes  $\overline{\text{PHIWRT}}$  (Write to PHI) or  $\overline{\text{BUFWR}}$  (Write to Buffer).

### 3.3 BUS DRIVERS.

- 3.3.1 A three-state octal buffer driver LS240 (U35) is used to transfer the data from the internal bus to the terminal data bus. It is selected by strobe  $\overline{\text{PHIRD}}$  (Read from PHI), or  $\overline{\text{BUFRD}}$  (Read from buffer).

### 3.4 BUFFER ADDRESS GENERATOR.

- 3.4.1 The buffer address generator includes two LS161 synchronous counters (U49,U58) used to generate the RAM's addresses A0 through A7.

The counters are incremented by the rising edge of  $\overline{\text{BUFWR}}$  or  $\overline{\text{BUFRD}}$  or  $\overline{\text{INCR.ADDR}}$ . The counters are reset to zero by  $\overline{\text{RSTBUF}}$ . The A0-7 addresses are read through a three-state octal buffer driver (U27) selected by strobe  $\overline{\text{BUFADR}}$  (Read Buffer Address).

### 3.5 BUFFER.

- 3.5.1 The buffer is made of three 1K RAMs (U28,U38,U48) organized as three 256 words by 4 bits each or 256 words by 12 bits for the complete buffer. Only eleven bits are used. In writing to the buffer 8 bits are coming via the data bus, and 3 bits via the address bus.

-----  
ADDR8, and ADDR3 are used to write bits D0 and D1 while ADDR7 writes the ENDBIT bit 11.  
When the transfer is from buffer to PHI, bit 11 is detected to terminate the transfer.

-----  
Strobe BUFWR (write to Buffer) or write Pulse from DMA are used to clock the data into the RAMs.

-----  
Strobe BUFRD or the write signal from DMA to PHI are used to enable the RAMs' outputs for buffer reading.

### 3.6 DMA.

3.6.1 The DMA is a state machine that allows the bidirectional transfer of data between the PHI chip and the RAM buffer in bursts. The DMA circuit includes an LS151 data selector/multiplexer (U59), an LS161 synchronous counter (U69), an LS42 4/10 line decoder (U610), and several gates and flip-flops.

3.6.2 At power on, the state machine is initialized to state 0. The PWR ON pulse also sets the LS279 latches. At other times, a command strobe -----  
RSTDMA does the same thing.

3.6.3 To initiate DMA action, command signals -----  
BUF2PHI or PHI2BUF is given to DMA. If the command is -----  
BUF2PHI, an LS279 latch (U510) is reset, its output inverted and an LS00 gate (U410) is enabled.

Either command strobes makes input D0 of LS151 (U59) high, thus allowing U69 to count one, being enabled by U57, Pin 8. This puts the state machine in state 1, the LS42 (U610) sets another LS279 latch (U510) and signal DMAACT goes true. DMAACT true selects the PHI chip, PHI chip's register 2 thru the LS157 data selector/multiplexer (U18) and also goes to the status register (U45). Also if U410, Pin 4 is enabled, the WRITE input of the PHI goes high, meaning a write operation to the PHI; otherwise, the WRITE input stays low, meaning a read operation. State 1 is an unconditional state, and DMA goes to state 2.

3.6.4 A DMA request from the PHI chip (DMARQ) lets the DMA go to state 3.

-----  
Entering state 3, signal IUGO2 is generated by an LS74 (U57) and the PHI chip is clocked. 100 nanoseconds after entering state 3, the output of another LS279 (U510) the write Pulse, goes low, because U610 is inhibited for the first 100 ns of each state by CLK at Pin 12.

As soon as the data is accepted by the PHI or its data out is valid at D0-D1, D8-15 inputs/outputs, the PHI chip outputs signal IOEND. When this occurs, the DMA moves to state 4. 100 nanoseconds after entering state 4, write pulse goes high, and if it is a write to buffer operation, the data from the PHI is clocked into the RAMs.

3.6.5 If this is not the last byte transferred or the buffer address generator has not reached 255, D4 of U59 is low, output W of U59 is high, and a paralleled load to state 1 is executed by the logic to the LS161 counter (U69). This cycle will be repeated until EOI or BUFFUL (buffer has reached 255) is detected.

3.6.6 Leaving state 4, signal  $\overline{\text{IUGO2}}$  goes false, signal  $\overline{\text{INCAADDR}}$  is generated at U47, Pin 8 and the buffer address is incremented by one. If EOI or BUFFUL is detected, D4A goes to state 5. 100 nanoseconds after entering state 5, an LS279 latch (U510) is reset and the signal  $\overline{\text{DCNE}}$  is generated interrupting the processor provided the INTERRUPT circuit (U23) is enabled. Then the DMA moves to state 6 which initiates a paralleled load to the LS161 (U69); returning the DMA to state 0; and setting the write latch (U510).  $\overline{\text{DMAACT}}$  goes false, and DMA stops.

### 3.7 EOI DECODER.

3.7.1 The EOI Decoder includes half an LS139 2/4 line decoder (U33) and and several gates. Bits D0 and D1 from the PHI are monitored by the LS139. The LS139 is enabled during a DMA transfer from PHI to buffer at  $\overline{\text{IUGO2}}$  time. When D0,D1 have the value 10 or 11, EOI becomes true and is applied to D4 of U59 to terminate the transfer, and to U55, Pin 13, the status register. If bits D0 and D1 have the value 01, secondary address indicator is decoded and sent to the status register U55, Pin 6.

When the DMA transfer is from buffer to PHI, the ENDHIT, bit 11 from the buffer is detected and sent to both the DMA and the status register as EOI.

### 3.8 PHI REGISTER ADDRESS MULTIPLEXER.

3.8.1 U18, the PHI register address multiplexer, is an LS157 quad 2-input multiplexer. It normally connects ADDR2, 1, 0 from the terminal's address bus to the PHI register address lines. When a DMA transfer is initiated, U18 is made to select PHI register 2 by  $\overline{\text{CHSEL2}}$  from DMA.

### 3.9 STATUS REGISTER.

3.9.1 The status register includes an LS174 hex D flip-flop (U55), and an LS242 three-state octal buffer driver (U45).

### 3.9.2 Status Interpretation:

Bit 7 is not used, and is always 0  
Bit 6, 1= DMA Active (DMAACT)  
Bit 5, 1= Buffer Full (BUFFUL)  
Bit 4, 1= End or Identify (Last Byte) EOI  
Bit 3, 1= Last Byte Type 1, (LSTPYT)  
Bit 2, 1= Secondary Address Indicator (SECADR)  
Bit 1, D0 (PHI chip bit 9)  
Bit 0, D1 (PHI chip bit 8)

The 6 lower bits are clocked into U55 by signals  $\overline{\text{IOG0}}$  ( $\overline{\text{IOG01}}$  or  $\overline{\text{IOG02}}$ ) or  $\overline{\text{BUFRD}}$  (processor read from buffer). The DMA status, bit 6 is always available thru U45. The Status register is read by the processor by strobing U45 with  $\overline{\text{IBSTAT}}$  (read status).

### 3.10 HP-IB ADDRESS.

- 3.10.1 The HP-IB address is a 5-position switch used to assign the HP-IB device address to which the PHI chip will respond when non-controller. Listen Always (S3-2) and Talk Always (S3-1) bits when set mean that the PHI chip is to assume that it is continuously addressed to listen or to talk or both. These switches are read by the processor by strobing U25 with  $\overline{\text{IBJMPR}}$ , (read jumpers).

### 3.11 INTERRUPT LOGIC.

- 3.11.1 Two signals can cause interrupt:  $\overline{\text{INT}}$  from the PHI or  $\overline{\text{DONE}}$  from DMA. Lines  $\overline{\text{ATN}}$  or  $\overline{\text{ATN2}}$  to the processor are switch selectable. The driver to either one of these two lines (U23) is normally disabled it is enabled by firmware thru U22, an LS74 D flip-flop, by clocking the flip-flop with "Send I/F Command" strobe "ANDed" with data bus bit 5= 1. If U23 is enabled, this will cause polling on the bus and U23, pin 3 will pull one of the BUS lines low. Which BUS line is pulled low is dependent on the "PL" switch setting.

### 3.12 HP-IB LOGICAL AND ELECTRICAL INTERFACING CIRCUIT.

- 3.12.1 This block includes a PHI (Processor to HP-IB Interface) chip (U210) and four quad three-state non-inverting transceivers (U111, U211, U311, U411) which together provide complete logical and electrical interface to the HP-IB as specified by IEEE Standard 488-1975. In addition, it provides buffering for inbound and outbound data through two FIFOs which can be accessed by the host processor.

- 3.12.2 The PHI chip appears to its processor as a bank of eight addressable registers. All interaction with the HP-IB is performed by reading or writing these registers. The capabilities they provide allow the host processor to connect to the HP-IB as a device responding to interface commands sent by a remote controller (computer, calculator, etc.) or, if desired, as the controller of the HP-IB.
- 3.12.3 The pins provided by the PHI chip for processor interfacing include the following:
- o a ten-bit wide data bus
  - o three register-select lines for selecting among the eight registers
  - o a data direction line to specify either reading or writing of the selected register
  - o two handshake lines to coordinate data transfer
  - o an interrupt line to alert the host processor of selected events
  - o a DMA-request line for use with external DMA facilities.
- 3.12.4 The eight addressable registers within the PHI chip perform the following functions:
- Register 0: INTERRUPTING CONDITIONS - A register which contains the values of nine interrupting status conditions plus a tenth bit which is the "OR" of the others. When this tenth bit has a "1" value, the host processor is interrupted by the PHI chip, assuming the proper interrupt enables are set up on the HP-IB PCA.
- Register 1: INTERRUPT MASK - A register whose bits are used to mask "OFF" (force to "0") corresponding bits of Register 0.
- Register 2: FIFO's - Two First-In-First-Out queues used for transferring bytes over the HP-IB. One FIFO is for inbound data transfer and the other is for outbound data transfer.
- Register 3: STATUS - A register which contains the values of non-interrupting internal chip status conditions.
- Register 4: CONTROL - A register which contains control bits accessible to the host processor which allow it to determine internal chip states.
- Register 5: ADDRESS - A register through which the host processor can inform the PHI which HP-IB address to use while communicating over the HP-IB, as well as a few other essentials.
- Register 6: PARALLEL POLL MASK/FIRST ID BYTE - Within an HP-IB controller, the bits of this register mask corresponding DIO line responses to a parallel poll. Within a non-controller, they are used as the first byte of a two-byte sequence which optionally can be used to identify the type of device which contains the PHI.

Register 7: PARALLEL POLL SENSE/SECOND ID BYTE - within an HP-IB controller, the bits of this register inform the PHI which assertion level is being used on each DIO line to indicate a need for service during a parallel poll. within a non-controller, they are used as the second byte of a two-byte sequence which can optionally be used to identify the type of device which contains the PHI.

NOTE: Soft reset (SRST) initializes to zero all registers except register 3.

### 3.12.5 Register 0: INTERRUPTS

	0	1	8	9	10	11	12	13	14	15	
Register	INT 1										1
Format :	PEND1 STATUS CONDITIONS CAUSING INTERRUPTS										1

Register 0 is provided for use by the host processor in identifying the cause of an interrupt generated by the PHI chip. Each bit in this register is associated with a particular interrupting condition as defined below but can be unconditionally forced to "0" (masked "OFF") over and above its definition by assigning a "0" value to the corresponding bit in Register 1 (INTERRUPT MASK). whenever a bit is masked "OFF", it also loses its ability to cause an interrupt of the host processor.

Bits 10 through 14 represent states of the chip. Unless they are masked "OFF" by Register 1, they are read as "1" values and continuously cause an interrupt condition as long as their associated states exist. writes to Register 0 have absolutely no effect on their values.

Bits 1, 8, 9, and 15 are set when particular events occur and are reset only when the host processor writes a "1" into their bit positions in Register 0. writes to Register 0 placing a "0" into their bit positions have no effect on their values. These bits are initialized to "0" whenever the Soft Reset (SRST) line is low.

Bit 0 - INTERRUPT PENDING: This bit is the logical "OR" of the nine low order bits after they are masked by corresponding bits of Register 1. whenever its value is still "1" after being masked by bit 0 of Register 1, the PHI provides a continuous interrupt to the host processor by grounding the INT line. writes to Register 0 affect the value of this bit only in as much as they change the value of the event recognition bits included in the "OR" function.

Bit 1 - PARITY ERROR: This bit becomes set whenever an interface command is received without odd parity. It is cleared when the host processor writes a "1" into its bit position.

- Bit 8 - STATUS CHANGE: This bit becomes set whenever there is a change in the value of the REMOTE bit in Register 3 while the PHI is a non-controller, or whenever there is a change in the value of the HP-IB CONTROLLER bit in Register 3. It is cleared when the host processor writes a "1" into its bit position.
- Bit 9 - PROCESSOR HANDSHAKE ABORT: This bit becomes set whenever there is a read from the inbound FIFO while it is empty or a write into the outbound FIFO while it is full (it does not get set within HP-IB controllers that have been conducting a parallel poll for at least 2 microseconds). If the host processor desires to repeat the read or write until it completes normally, the PHI chip guarantees that data will not be lost. This bit is cleared when the host processor writes a "1" into its bit position.
- Bit 10 - PARALLEL POLL RESPONSE for HP-IB controllers only: A "1" value in this bit position indicates that a parallel poll is being conducted and one or more devices are indicating a need for service. Specifically, this interrupt occurs as long as all of the following are true:
- 1) The outbound FIFO is empty and hence a parallel poll is being performed.
  - 2) The parallel poll has been performed for at least 2 microseconds to provide time for the bus DIO lines to settle.
  - 3) The inbound FIFO is also empty so that the host processor will not obtain data when it reads from Register 2 in response to this interrupt.
  - 4) One of the devices on the HP-IB is indicating a need for service by asserting a DIO line which has been masked "ON" by Register 6 (the level of assertion depends on the corresponding bit in Register 7).
- Bit 11 - SERVICE REQUEST for HP-IB Controllers only: A "1" value in this bit position indicates that one or more devices are requesting service via the bus SRO line.
- Bit 12 - FIFO ROOM AVAILABLE: A "1" value in this bit position indicates that the outbound FIFO is not full and can accept writes without aborting.
- Bit 13 - FIFO BYTES AVAILABLE: A "1" value in this bit position indicates that the inbound FIFO contains one or more bytes which can be read by the host processor.

Bit 14 - FIFO IDLE: A "1" value in this bit position indicates that the outbound FIFO is empty. within HP-IB controllers, this situation always causes a continuous parallel poll to be performed.

Bit 15 - DEVICE CLEAR: This bit becomes set whenever a "Device Clear" interface command is received via the HP-IB while the PHI is a non-controller. while it is set, it blocks all transfer between the FIFO's and the HP-IB so that they can be cleared by the host processor without losing subsequent data. The host processor can then clear this bit by writing a "1" into its bit position.

### 3.12.6 Register 1: INTERRUPT MASK

	0	1	8	9	10	11	12	13	14	15	
Register	INT 1										1
Format :	IEVAB1										1
	INTERRUPT MASK BITS										

A "0" value in any bit position of Register 1 causes the corresponding bit in Register 0 to always read as "0" and prevents that bit from causing an interrupt to the host processor. Since the INTERRUPT ENABLE (INT ENAB) bit can hold off all interrupts by directly masking bit 0 in Register 0, the host processor can view all interrupting conditions without getting an interrupt by setting it to "0" and setting all other mask bits to "1".

Register 1 can be read or written by the host processor at any time and is initialized to all zeros whenever the soft reset (SRST) line is low.

### 3.12.7 Register 2 write: OUTBOUND FIFO

Each write into Register 2 causes a word to be placed into an 8-word-long outbound FIFO queue. This FIFO holds data bytes waiting to be sent over the HP-IB to other devices. Within HP-IB controllers, it is also used to hold interface commands as well as control words which regulate the sending of data bytes by other devices on the HP-IB.

If the outbound FIFO is full during any attempt to write into it, the handshake with the host processor will be completed without destroying any data already in the FIFO, and the PROCESSOR HANDSHAKE ABORT bit (bit 9) in Register 0 will be set. An aborted attempt to write into the outbound FIFO can be repeated if desired until the word is finally accepted by the PHI.

As each word reaches the HP-IB end of the outbound FIFO, it is interpreted by the PHI to allow one or more bytes to be transferred over the HP-IB. It is automatically removed from the FIFO at the completion of this transfer allowing the next word in sequence to be interpreted.



If a non-controlling device containing a PHI chip is addressed to talk and is expected to send data bytes but its outbound FIFO is empty, the HP-IB will remain idle until the host processor places a data byte into the FIFO. If either the DATA FREEZE bit in Register 3 or the DEVICE CLEAR bit in Register 0 is set, the PHI will refuse to send data bytes, even if they exist in the outbound FIFO, until the host processor resets that bit.

Within an HP-IB controller, the DATA FREEZE and DEVICE CLEAR bits cannot become set. However, if either bit happens to be already set within a device at the time it becomes the HP-IB controller, the PHI will not allow any byte transfer over the HP-IB until the host processor resets that bit.

When the outbound FIFO within an HP-IB controller is empty, the PHI chip automatically conducts a continuous parallel poll on the HP-IB. This poll terminates as soon as the next word is placed into the outbound FIFO by the host processor. THE PARALLEL POLL RESPONSE interrupt (bit 10 in Register 0) is provided to alert the host processor that at least one device is indicating a need for service during this poll.

The PHI provides two interrupts for the host processor to help it coordinate outbound FIFO activity. One indicates when the FIFO contains room for more words to be written into it, and the other indicates when it is completely empty.

The outbound FIFO is initialized to an empty state when the soft reset inout pin is set to a low value and also whenever a "1" is written into the INITIALIZE OUTBOUND FIFO bit (bit 15) in Register 4.

If, within an HP-IB controller, the INITIALIZE OUTBOUND FIFO bit is used at a time when the ATN line is false on the HP-IB, it will force the ATN line to be asserted asynchronously, possibly while a data byte is being sent, causing one or more devices to see a "phantom" interface command. Since this situation requires that the HP-IB controller bring all HP-IB devices to a known state by sending a long string of interface commands, it should be avoided wherever possible. At all other times that ATN is asserted by the PHI, its assertion is synchronized with the preceding data transfer, effectively eliminating the chance of "phantom" interface commands.

Within a non-controlling device, all words written into the outbound FIFO contain a single data byte to be sent over the HP-IB. Within an HP-IB controller, however, a word written into the outbound FIFO can be one of three choices:

- 1) a DATA BYTE to be sent over the HP-IB,
- 2) an INTERFACE COMMAND to be sent over the HP-IB,

or 3) a BYTE TRANSFER ENABLE to allow another device to send bytes over the HP-IB.

#### OUTBOUND FIFO

	0	1	8	9	10	11	12	13	14	15
DATA BYTE:	DATA BYTE VALUE									

When a DATA BYTE code reaches the HP-IB end of the outbound FIFO, it is sent over the HP-IB along with its associated END bit value to all currently addressed listeners.

Within a non-controlling device, data bytes are sent over the HP-IB only if the device is addressed to talk and the HP-IB controller has allowed byte transfer to take place. If these two conditions are not met when a data byte reaches the end of the FIFO, it waits there until they are.

Within an HP-IB controller, the data byte will be sent over the HP-IB as soon as it reaches the end of the FIFO. However, the host processor must guarantee that it is addressed to talk at this time and not in serial poll mode. Otherwise, the DATA BYTE code will be erroneously interpreted as a BYTE TRANSFER ENABLE. If an HP-IB controller addresses itself to listen to its own data bytes, the high-order bits (D0 and D1) added to the byte as it wraps around into the Inbound FIFO will be undefined (they will not contain the normally defined last byte information).

#### OUTBOUND FIFO

	0	1	8	9	10	11	12	13	14	15
INTERFACE COMMAND:	INTERFACE COMMAND CODE									

For HP-IB controllers only: When this word reaches the HP-IB end of the outbound FIFO, the interface command byte is sent over the HP-IB to all devices on the bus. During this transfer, the PHI chip automatically sets the value of DIO8 to generate odd parity on the HP-IB.

BYTE TRANSFER ENABLE: (HP-IB controllers only)

	0	1	8	9	10	11	12	13	14	15
COUNTED TRANSFER ENABLE:	BYTE COUNT									

	0	1	8	9	10	11	12	13	14	15
UNCOUNTED TRANSFER	1	1	1	1		0				1
ENABLE:	1	1	1							1
(see note 2)										

After addressing another device to talk, the host processor should place a BYTE TRANSFER ENABLE into its own outbound FIFO to remove the ATN signal from the HP-IB and allow bytes to be sent to all addressed listeners. The PHI will automatically terminate this transfer when:

- 1) a byte is sent with its accompanying END bit set,
- 2) an ASCII line feed character (hex 0A) is sent during a counted transfer whose LF INH (Line Feed Inhibit) bit is "0",
- or 3) the number of bytes specified by a BYTE COUNT field have been sent (an all-zero BYTE COUNT field is used to specify a 256-byte transfer).

An HP-IB controller must guarantee that either it is not addressed to talk or it is in serial poll mode when a BYTE TRANSFER ENABLE reaches the end of the FIFO. Otherwise, it will be erroneously interpreted as a DATA BYTE.

Notes:

- 1) An HP-IB controller can also use a BYTE TRANSFER ENABLE to obtain its own serial poll response byte or identification code bytes if desired for self diagnostics.
- 2) If bits 8 through 15 of an UNCOUNTED TRANSFER contain a non-zero value, they will be interpreted as a BYTE COUNT field and counting will be performed in spite of the high-order "11" code. This interpretation is for backwards compatibility only and is redundant with part of the COUNTED TRANSFER's capability. This code should not be used for new software design.

### 3.12.8 Register 2 Read: INBOUND FIFO

Each read from Register 2 retrieves one word from an 8-word-long inbound FIFO queue. This FIFO is used by the PHI to hold data bytes and secondary addresses which have arrived from the HP-IB and are waiting to be read by the host processor.

If the inbound FIFO is empty during any attempt to read from it, one of the following two situations will occur:

- 1) If the device containing the PHI chip is the HP-IB controller and has been conducting a parallel poll for at least 2 microseconds (the outbound FIFO has been empty for at least 2 microseconds), then the read from Register 2 will obtain the DIO line responses of the eight polling devices, masked and normalized by Registers 6 and 7. This word will have the following format:

	1	0	1	1	8	1	9	1	10	1	11	1	12	1	13	1	14	1	15	1
PARALLEL	-----																			
POLL	1	0	1	0	1	DIO	DIO	DIO	DIO	DIO	DIO	DIO	DIO	DIO	DIO	DIO	DIO	DIO	DIO	1
RESPONSES:	1	1	1	8	7	6	5	4	3	2	1									
	-----																			

It is recommended that the host processor attempt to obtain these responses only when servicing the provided PARALLEL POLL RESPONSE interrupt.

- 2) In all other cases, the read from Register 2 will obtain a word of indeterminate value and the HANDSHAKE ABORT bit (bit 9) in Register 0 will be set.

An aborted attempt to read from the inbound FIFO can be repeated if desired, until a valid word is finally obtained.

Data bytes enter the inbound FIFO from the HP-IB only if the device containing the PHI is addressed to listen while they are being sent. Secondary addresses enter the inbound FIFO only if the preceding interface command sent over the HP-IB was the device's primary talk or listen address.

If the PHI chip is in the process of receiving a data byte or a secondary address from the HP-IB but either the inbound FIFO is full or the DEVICE CLEAR bit in Register 0 is set, it will hold off the HP-IB handshake until the host processor reads a word from the FIFO or clears the DEVICE CLEAR bit. An interrupt is provided by the PHI to notify the host processor when the inbound FIFO contains one or more words for it to read.

The inbound FIFO is initialized to an empty state only when the soft reset input pin has a low value.

When a word enters the inbound FIFO, its high order two bits (D0,D1) are set to indicate whether it is a secondary address, a standard data byte, or the last data byte of a record or requested sequence. The following pages describe in greater detail the formats of these entry types.

	0	1	8	9	10	11	12	13	14	15	
	-----										
DATA BYTE:	1	0	1	0	DATA BYTE VALUE						1
	-----										

This format is used for any received data byte which is not the last byte of a subgroup or record as defined below.

	0	1	8	9	10	11	12	13	14	15	
LAST BYTE OF SUBGROUP:	1	1	0	1	DATA BYTE VALUE						1

This format is used only within HP-IB controllers for a data byte which caused the byte count of a BYTE TRANSFER ENABLE to expire, but which is not the last byte of the record as defined below.

	0	1	8	9	10	11	12	13	14	15	
LAST BYTE OF RECORD:	1	1	1	1	DATA BYTE VALUE						1

This format is used for a received data byte which is the last byte of a record and will occur in two cases:

- 1) the END bit which accompanied the data byte on the HP-IB was set to "1"

or 2) within HP-IB controllers only, the data byte is an ASCII line feed character that was received in response to a BYTE TRANSFER ENABLE which requested line feed detection.

	0	1	8	9	10	11	12	13	14	15	
SECONDARY ADDRESS:	1	0	1	1	0	0	1	TLK	SECONDARY ADDRESS		

This format contains the 5-bit address field (DIO5-DIO1) of a secondary talk address or secondary listen address to instruct a device to participate in the next byte transfer, it can send a secondary talk or listen address to further define the source or destination of the bytes within the device. When a PHI chip receives a secondary address from the HP-IB controller, it is placed into the inbound FIFO for evaluation by the host processor.

The TLK bit is set to "1" if the preceeding primary interface command was the talk address of the device containing the PHI. The TLK bit is set to "0" if the preceeding primary interface command was the device's listen address (see section 4.0).

### 3.12.9 Register 3: STATUS

	0	1	8	9	10	11	12	13	14	15
Register	----	----	----	----	----	----	----	----	----	----
Format :	///	///	HI ORDER	REM	HPIB	SYST	TLK	LTN	DATA	
	///	///	ACCESS		CTRL	CTRL	IDF		FRZ	

Register 3 can be read at any time by the host processor to obtain the values of eight status conditions within the PHI chip. A write into this register can affect only bits 8, 9, and 15 as defined below.

Bits 0, 1 - UNASSIGNED: Always has "0" value when read.

Bits 8, 9 - HIGH-ORDER BIT ACCESS: These bits are intended to act as a substitute for pins D0 and D1 in applications where only an 8-bit data path is available for communication between the PHI and its host processor. Whenever any PHI register other than Register 3 is read by the host processor, these two bits are set to the values being sent out of the PHI on pins D0 and D1 for later access by the processor. Reading from Register 3 causes no change in the value of these bits.

Conversely, if the "8-BIT PROCESSOR" bit in Register 4 is set while any PHI register other than Register 3 is being written into by the host processor, these two bits are used instead of pins D0 and D1 as the source of high-order bit data into that register.

These bits can be altered directly by a write to Register 3 and, if bit 15 is written as a zero, this write operation will have no other effect on the state of the PHI chip. These bits are useful in some 10-bit data path applications since they provide a "second chance" to access the high-order bits of the inbound FIFO after a read from Register 2.

Bit 10 - REMOTE: This bit has a "1" value if the device containing the PHI chip is in the remote state as defined by the HP-IB Standard. It is mainly for use within instruments which can be programmed either from their front panel or via the HP-IB.

Bit 11 - HP-IB CONTROLLER: This bit has a "1" value whenever the device containing the PHI is the current HP-IB controller.

It becomes set when any of the following conditions are met:

- 1) A "Take Control" interface command is received from the current HP-IB controller.
- 2) (within System Controllers only)- The IFC line of the HP-IB is asserted.

It becomes cleared when any of the following conditions are met:

- 1) The PON input pin (SRST) is brought low.
- 2) The PHI goes from "offline" to "online" state.
- 3) A "Take Control" interface command is sent by the PHI to another device on the HP-IB.
- 4) (within non-System Controllers only)- The IFC line of the HP-IB is asserted.

- Bit 12 - HP-IB SYSTEM CONTROLLER: This bit has a "1" value when the device containing the PHI is the system controller of the HP-IB (its SCKRL pin is high) or when the PHI is offline.

The HP-IB system controller is the only device in a system that can assert the IFC or REN lines of the HP-IB.

When a device is offline, the IFC and REN lines are asserted only within the PHI and not on the actual HP-IB. This feature is very useful in offline diagnostics since it allows any device to set IFC while it is offline to locally become its own HP-IB controller. It can then send itself interface commands and test its response to them offline without interfering with the operation of the real HP-IB.

- Bit 13 - ADDRESSED TO TALK OR IDENTIFY: This bit has a "1" value whenever the device containing the PHI is addressed to talk or to send identification bytes over the HP-IB, whether or not a serial poll is being conducted.

- Bit 14 - ADDRESSED TO LISTEN: This bit has a "1" value whenever the device containing the PHI is addressed to listen to bytes sent over the HP-IB.

Bit 15 - OUTBOUND DATA FREEZE: This bit becomes set within a non-controlling device whenever a byte enters its inbound FIFO from the HP-IB (not from its own outbound FIFO). While it is set, it prevents data from leaving the outbound FIFO over the HP-IB to give the host processor a chance to read the byte which arrived and possibly change its mind about sending any data which is already in the outbound FIFO. The host processor can reset this bit by writing a "1" into its bit position, but only if the inbound FIFO is empty (eg. no other byte has arrived from the HP-IB).

### 3.12.10 Register 4: CONTROL

```

Register      | 0 | 1 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
Format :      |---|---|---|---|---|---|---|---|---|---|
                |///|///|8BIT|PRJY|REN|IFC|RSPD|RQST|FIFO|INIT|
                |///|///|PROC|FRZ |  |  |  |POLL|SRVC|SEL |FIFO|

```

Register 4 can be read or written at any time by the host processor to access eight control bits within the PHI Chip. All bits are initialized to zero by soft reset (SRST) (pin 15 is pulsed low). The control bits are defined as follows:

Bit 0 - RESERVED: This bit always has a "0" value when read and must never be written as a "1".

Bit 1 - RESERVED: This bit always has a "0" value when read and must never be written as a "1".

Bit 8 - 8 BIT PROCESSOR: A "1" value in this bit position indicates to the PHI that the host processor wishes to use an 8-bit data path instead of the standard 10-bit one. Specifically, during a write to any register except Register 3, the PHI uses the current values of bits 8 and 9 of Register 3 instead of data which would normally arrive via the D0 and D1 lines. D0 and D1 can be left untied if only 8-bit communication is desired (the "8 BIT PROCESSOR" bit is always set). However, during reads from the PHI, D0 and D1 always contain valid high-order bit values, even if the "8 BIT PROCESSOR" bit is set, and may prove useful in some applications.

Bit 9 - PARITY FREEZE: whenever this bit has a "1" value, the PHI chip will refuse to accept or interpret any interface command (including device addresses) that does not have ODD parity. This will force the HP-IB to remain frozen with DAV asserted and the erroneous interface command held on the bus DIO lines until the HP-IB controller aborts the transfer by removing DAV. This bit does not affect in any way the "PARITY ERROR" interrupt bit in Register 0.



- Bit 10- REN VALUE (System controllers only): If the device containing the PHI is system controller of the HP-IB, this bit determines the value of the bus REN line.

WHENEVER THIS LINE IS ASSERTED, IT MUST REMAIN ASSERTED FOR AT LEAST 100 MICROSECONDS TO MEET IEEE STD 488-1975 SPECIFICATIONS

A system controller can assert the REN line at any time to allow programmable instruments tied to the HP-IB to be remotely programmed in lieu of their front-panel controls.

When the PHI is "offline", this bit can be used locally in diagnostics whether or not the device is a system controller.

- Bit 11- IFC VALUE (System controllers only): If the device containing the PHI is system controller of the HP-IB, this bit determines the value of the bus IFC line.

WHENEVER THIS LINE IS ASSERTED, IT MUST REMAIN ASSERTED FOR AT LEAST 100 MICROSECONDS TO MEET IEEE STD 488-1975 SPECIFICATIONS

A system controller can assert the IFC line at any time to initialize the HP-IB interfaces within all devices connected to the HP-IB (note that the devices themselves are not initialized - only their HP-IB interfaces). Assertion of this line also has the effect of forcing the system controller to be the HP-IB controller no matter which device previously had this capability (see discussion of HP-IB controller bit in Register 3). As a result, the system controller need not follow the normal "Take Control" interface command protocol when it wishes to regain control of the HP-IB after it has passed it away or when it has just gone "online".

When the PHI is "offline", this bit can be used locally in diagnostics whether or not the device is a system controller.

- Bit 12- RESPOND TO PARALLEL POLL: whenever this bit has a "1" value, the PHI chip will indicate a need for service during any parallel poll if it has parallel poll response capability (see discussion of HP-IB ADDRESS in Register 5 description).

- Bit 13- REQUEST SERVICE: whenever this bit has a "1" value, the PHI chip will use the HP-IB SRQ line and serial poll facility to request service from the HP-IB controller in accordance with the rules of the HP-IB Standard:

- 1) It begins asserting the SRQ line as soon as this bit is set.
- 2) when it is first polled by the HP-IB controller during a serial poll, it stops asserting the SRQ line and responds to

this poll and all subsequent ones with a hex "40" (DIO7= 1).

3) The host processor should keep this bit set until service is obtained from the HP-IB controller.

4) After the host processor clears this bit, the PHI will respond to all serial polls with a hex "80" (DIO7= 0 and odd parity).

Bit 14- DMA FIFO SELECT: Whenever this bit has a "1" value, the <sup>-----</sup>DMA<sub>REQ</sub> pin of the PHI chip will be asserted (low) whenever the outbound FIFO is ready for a write operation. If this bit has a "0" value, the <sup>-----</sup>DMA<sub>REQ</sub> pin will be asserted whenever the inbound FIFO is ready for a read operation.

Bit 15- INITIALIZE OUTBOUND FIFO: Any time a "1" value is written into this bit position, the outbound FIFO will be forced empty (but not necessarily unfrozen - see Register 3 bit 15). No actual storage location corresponds to this bit position and it always has a "0" value when read.

### 3.12.11 Register 5: HP-IB ADDRESS

	0	1	8	9	10	11	12	13	14	15
Register	-----									
Format :										

Register 5 can be read or written at any time by the host processor to specify an HP-IB address and related control information to the PHI.

All bits in this register are initialized to zero whenever the soft reset (SRST) line is low.

Bit 0 - RESERVED: This bit always has a "0" value when read and must never be written as a "1".

Bit 1 - RESERVED: This bit always has a "0" value when read and must never be written as a "1".

Bit 8 - ONLINE: Whenever this bit has a "1" value, the PHI chip is "online" and will interact normally with the HP-IB. If it is "0", the PHI chip is "offline" and will not interact in any way with the HP-IB. When this bit becomes set, the PHI waits for a

<sup>----</sup>period equal to the width of IOGO before actually going online. During this period, the PHI initializes its interface circuitry to the HP-IB so that it does not start out as a talker, listener or controller (this performs the function of the "pon"

message defined in the Interface Standard). If other bits in Register 5 were set simultaneously with the ONLINE bit, they are also given a chance to settle during this time.

- Bit 9 - TALK ALWAYS: This bit is included for communication between devices in systems without a controller and should not be set when a controller is present except in diagnostics. When it is set, the PHI chip assumes that it is continually addressed to talk unless the bus IFC line is being asserted. When it is cleared by the host processor, the PHI continues to be addressed to talk until the IFC line is asserted, the talk address of another device is received, or the soft reset (SRST) line is brought low.
- Bit 10- LISTEN ALWAYS: This bit is included for communication between devices in systems without a controller and should not be set when a controller is present except in diagnostics. When it is set, the PHI chip assumes that it is continually addressed to listen unless the bus IFC line is being asserted. When it is cleared by the host processor, the PHI continues to be addressed to listen until the IFC line is asserted, the unlisten command is received, or the soft reset line is brought low.
- Bits 11-15 - HP-IB ADDRESS: within a non-controlling device, the values of these five bits determine the HP-IB address to which the PHI chip will respond. Any address between 0 and 29 can be used but addresses 30 and 31 should be avoided. If the address specified is between 0 and 7, the PHI chip will assume that it can respond to parallel polls initiated by the HP-IB controller and will use a DIO line corresponding to its address (DIO8 through DIO1 correspond with address 0 through 7 respectively). The other addresses are not assigned initial parallel poll response capability but may be dynamically assigned it by the HP-IB controller.

Within an HP-IB controller, the PHI always responds to Address 30 for talking and listening, not to the address specified by these bits. This feature allows constants to be used for self-addressing within controller software.

### 3.12.12 Register 6: PARALLEL POLL MASK/FIRST ID BYTE

	0	1	3	9	10	11	12	13	14	15
Register	-----									
Format :	1///1///1 MASK BITS/FIRST ID BYTE									
	-----									

Register 6 can be read or written at any time within an HP-IB controller to provide a mask for incoming parallel poll responses. Within a

non-controlling device, it is used by the host processor to specify the first byte of a two-byte product type Identification Code as defined below. All bits are initialized to "0" whenever the Soft Reset (SRST) input has a low value.

WITHIN AN HP-IB CONTROLLER:

Each bit in this register which has a "0" value masks "OFF" (forces to zero) the parallel poll response arriving via its corresponding DIO line whenever a parallel poll is being conducted (see the description of Register 7 for information on how the responses are actually derived from the DIO line values). Only those responses which are not masked "OFF" are included in the determination of the PARALLEL POLL RESPONSE interrupt.

WITHIN A NON-CONTROLLING DEVICE:

This register and Register 7 can optionally participate in an identification sequence through which the HP-IB controller can find out what type of device exists at each HP-IB address.

if it is desired to use this feature, the host processor should perform the following set-up:

- 1) Before going online, Registers 6 and 7 should be loaded with a 16-bit device type Identification Code assigned to the product and the "RESPOND TO PARALLEL POLL" bit in Register 4 should be set.
- 2) The PHI should be placed online while the "RESPOND TO PARALLEL POLL" bit is still set, causing it to indicate a need for service during any parallel poll conducted by the HP-IB controller.
- 3) After the HP-IB controller has acknowledged that it has seen the parallel poll response, the "RESPOND TO PARALLEL POLL" bit can be cleared.

After the above set-up has been performed, circuitry within the PHI is enabled to allow it to respond to a special primary/secondary address pair separate from its normal HP-IB address, without any interaction with the host processor. Whenever the PHI receives Talk Address 31 followed by a secondary address containing the 5-bit HP-IB ADDRESS specified in Register 5, it will send first the contents of Register 6 and then the contents of Register 7 as data bytes, marking the contents of Register 7 with an accompanying END bit as it is sent (the secondary addressing used obeys all the rules of an "Extended Talker" defined in the HP-IB Standard).

If this feature is not desired, the "RESPOND TO PARALLEL POLL" bit should have a "0" value at the time the PHI goes online. This causes all of the special address pair recognition circuitry to be disabled.

### 3.12.13 Register 7: PARALLEL POLL SENSE/SECOND ID BYTE

	0	1	8	9	10	11	12	13	14	15
Register	-----									
Format :	SENSE BITS/SECOND ID BYTE									
	-----									

Register 7 contains 8 bits which can be read or written at any time within an HP-IB controller to specify the assertion levels of the incoming parallel poll responses. Within a non-controlling device it is used by the host processor to specify the second byte of a two-byte product type Identification Code as defined below. All bits are initialized to "0" whenever the Soft Reset (SRST) line has a low value.

#### WITHIN AN HP-IB CONTROLLER:

Each bit in this register is "EXCLUSIVE-OR"ed with the parallel poll response arriving via its corresponding DIO line whenever a parallel poll is being conducted. A particular bit should be set to "1" only if it is known that the device responding via its corresponding DIO line is using a "0" value to indicate its need for service.

(Multiple devices can be programmed to use a "0" value on the same DIO line to indicate readiness for some operation and the controller will see the interrupt only after they are all ready).

#### WITHIN A NON-CONTROLLING DEVICE:

This register and Register 6 can optionally participate in an identification sequence through which the HP-IB controller can find out what type of device exists at each HP-IB address.

Complete details of this sequence are contained in the description of Register 6.

### 3.12.14 OFF LINE DIAGNOSTICS

As long as bit 8 of Register 0 has a "0" value, the PHI remains offline (this is also the state to which the PHI is initialized). While the PHI is off-line, it is completely isolated from the HP-IB and its circuitry can be diagnosed by the host processor without interfering with normal HP-IB operation.

Although the PHI is isolated from the external HP-IB, its complete set of interface functions are still tied together internally and interact normally with each other via an internal copy of the HP-IB. It is important to note here that the circuitry used to do this is not special "off-line circuitry" but the same circuitry used when the PHI is on-line. All timing and sequencing will satisfy not only data sheet specifications but also all HP-IB regulations.

Most diagnostics which can be performed off-line require that the PHI be the controller of its internal HP-IB so that it can send itself interface commands. Since only an HP-IB system controller can use the IFC line to take control of the HP-IB, an off-line PHI will assume system controller status in spite of the value of its "SCTRL" pin.

In order to test the FIFOs within an off-line PHI, for example, a host processor can take control of the internal HP-IB and send its own talk and listen addresses via the outbound FIFO. Once this has been done, all data bytes sent out through outbound FIFO will wrap around via the internal HP-IB into the inbound FIFO for validity checking by the host processor. Secondary addresses, parallel poll responses, and identification bytes can also be read through the inbound FIFO to be checked for validity.

### 3.12.15 HP-IB COMPATIBILITY LEVELS

The following is a list of interface function subsets implemented by this HP-IB Interface Module. The full definition is given in the IEEE 488-1975 document standard.

SOURCE HANDSHAKE: SH1

ACCEPT HANDSHAKE: AH1

TALKER # 1: T1  
(used for all data transfer)

TALKER # 2: TE4  
(Primary Address = 31, used for device identification bytes)

LISTENER: L1

SERVICE REQUEST: SR1  
(STB message is set by PHI to all zeros)

REMOTE/LOCAL: RL1

PARALLEL POLL: PP1  
("lpe" is not excluded until the first PPE, PPD, or PPU is received)

DEVICE CLEAR: DC1

CONTROLLER: C1, C2, C3, C4, C5

## 4.0 HP-IB INTERFACE COMMANDS

### 4.0.1 PRIMARY COMMAND GROUP:

Interpretation of these commands depends on the values of bits 7 thru 1.

ADDRESSED COMMANDS:		8	7	6	5		4	3	2	1	
		X	0	0	0		CMD. CODE				

#### COMMAND CODE:

0001: GO TO LOCAL  
0100: SELECTED DEVICE CLEAR  
0101: PARALLEL POLL CONFIGURE  
1000: GROUP EXECUTE TRIGGER  
1001: TAKE CONTROL \*

\*(Interpreted only by the device addressed to talk. All other addressed commands are interpreted only by the device(s) addressed to listen).

UNIVERSAL COMMANDS:		8	7	6	5		4	3	2	1	
		X	0	0	1		CMD. CODE				

#### COMMAND CODE:

0001: LOCAL LOCKOUT  
0100: DEVICE CLEAR \*  
0101: PARALLEL POLL UNCONFIGURE  
1000: SERIAL POLL ENABLE  
1001: SERIAL POLL DISABLE

\*(Does not clear the current controller).

LISTEN ADDRESSES:		8	7	6		5	4	3	2	1	
		X	0	1		DEVICE ADDRESS					

(Device address must not be 11111)

UNLISTEN COMMAND:		8	7	6		5	4	3	2	1	
		X	0	1		1	1	1	1	1	

TALK ADDRESSES:	8	7	6	5	4	3	2	1
	X	1	0	DEVICE ADDRESS				

#### ADDRESS CODE:

31(decimal) = identify if 1DF flip-flop is set, else a normal address.

#### 4.0.2 SECONDARY COMMAND GROUP:

Interpretation of one of these commands depends on the values of bits 5 through 1 and on the primary interface command sent prior to it.

SECONDARY LISTEN ADDRESS:	8	7	6	5	4	3	2	1
	X	1	1	DEVICE ADDRESS				

(Sent following a listen address and is interpreted only by the devices recognizing the preceeding listen address. It is used to distinguish among 32 devices all with the same listen address or to distinguish among registers of a single device).

SECONDARY TALK ADDRESS:	8	7	6	5	4	3	2	1
	X	1	1	DEVICE ADDRESS				

(Sent following a talk address and is interpreted only by the device recognizing the preceeding talk address. It is used to distinguish among 32 devices all with the same talk address or to distinguish among registers of a single device).

PARALLEL POLL ENABLE:	8	7	6	5	4	3	2	1
	X	1	1	0	S	LINE NBR.		

(Sent following a parallel poll configure and is interpreted only by device(s) which were addressed to listen when parallel poll configure was sent. LINE NBR. tells the device(s) which DIO line to use to respond to future polls and the S (Sense) bit tells it which way to pull the line to indicate an interrupt).



PARALLEL POLL  
DISABLE:

8	7	6	5	4	3	2	1
X	1	1	1	X	X	X	X

(Sent following a parallel poll configure and is interpreted only by device(s) which were addressed to listen when parallel poll configure was sent).

## 5.0 PHI CHIP SYMBOLS DESCRIPTIONS

P/N	SYMBOL	NAME	DESCRIPTION
1	SCRTL	System Controller	When asserted, this input provides the chip with system control capabilities as defined by the HP-IB Standard (i.e. it can drive the HP-IB's IFC and REN lines). Only one device in any system should have this pin asserted.
2	DAV	Data Valid	This bidirectional pin ties to the HP-IB DAV line via an MC3448 transceiver.
3	EOI	End or Identify	This bidirectional pin ties to the HP-IB EOI line via an MC 3448 transceiver.
4-11	DIO8-1	Data I/O Bit 8 through Bit 1	These bidirectional pins tie to the HP-IB DIO lines via eight MC3448 transceivers.
12	VDD	Power Supply Pin	Supplies 12V to the chip.
13	RS	Delay Stabilizing Resistor	This pin should be tied to ground through a resistor whose value is 26.1Kohms +/- 1%.
14	DMARQ	DMA Request	This output can be used to request DMA cycles to transfer data to the outbound FIFO or from the inbound FIFO.
15	SRST	Soft Reset	This input when pulsed low for at least 500 ns will cause all circuits within the PHI chip to be initialized.

16	WRITE	Write	This input when asserted specifies that a WRITE rather than READ operation is being performed by the processor.
17	INT	Interrupt	This output provides a level which should be used to interrupt the host processor.
18	IOEND	I/O END	This output is used to handshake all chip reads and writes within asynchronous systems. It can be ignored within synchronous systems
19	IOGO	I/O GO	This input is used to cause a read from or a write to a specified register within the chip. It is ignored if the Chip Select input is not asserted.
20-22	ADDR2-0	Address Bits 2 thru 0	These inputs are used to specify the number of a register being read from or written to. Address 2 is the high order bit.
23	CHSEL	Chip Select	When this input is asserted, it allows the chip to respond to read or write cycles initiated by the processor via the IOGO line.
24	VDC	Power Supply Pin	Supplies +5 volts to the chip.
25-34	D0-15	Processor Data Bits 0,1,8-15	These bidirectional pins carry data during reads from or writes to the chip by the host processor. D0 and D1 are used only for registers 0,1 and 2 and remain at high impedance during reads of register 3, 4, 5, 6, or 7.
35	RTL	Return to Local	This input carries the "rtl" message for the REMOTE/LOCAL interface function as defined in IEEE 488-1975. This function is not used on this interface PCA and therefore is tied low.
36	GND	Ground	Ground used for all power supply pins.

37	TRIG	Trigger	This output is not used on this interface. PCA.
38	--- ATN	----- Attention	This bidirectional pin ties to the HP-IB ATN line via an MC3448 transceiver.
39	--- SRQ	----- Service Request	This bidirectional pin ties to the HP-IB SRQ line via an MC3448 transceiver.
40	RFD	Ready for Data	This bidirectional pin ties to the HP-IB NRFD line via an MC3448 transceiver.
41	DAC	Data Accepted	This bidirectional pin ties to the HP-IB NDAC line via an MC3448 transceiver.
42	--- REN	----- Remote Enable	This bidirectional pin ties to the HP-IB REN line via an MC3448 transceiver.
43	--- IFC	----- Interface Clear	This bidirectional pin ties to the HP-IB IFC line via an MC3448 transceiver.
44	CIC	Controller In Charge	This output is asserted when the host device is the Controller-In-Charge of the HP-IB. It is used as an enable for the ATN line driver. If CIC is false the SRQ driver will be enabled instead.
45	HSE	High State Enable	This line is asserted whenever the DIO, DAV, or EOI lines are required to have active pullups if they are driving a high level. It should be tied to the high state enable inputs of the corresponding MC3448 transceivers.
46	DEE	DAV/EOI Enable	When asserted, this output enables the DAV and EOI MC3448 drivers. When it is unasserted, it enables the RFD and DAC line drivers.
47	DIOE	DIO Enable	This output, when asserted, enables the eight DIO MC3448 drivers
48	VCC	Power Supply Pin	Supplies +5 volts to the chip.

## 6.0 HP-IB DRIVERS

See attachment 1 for HP-IB drivers sample listing.

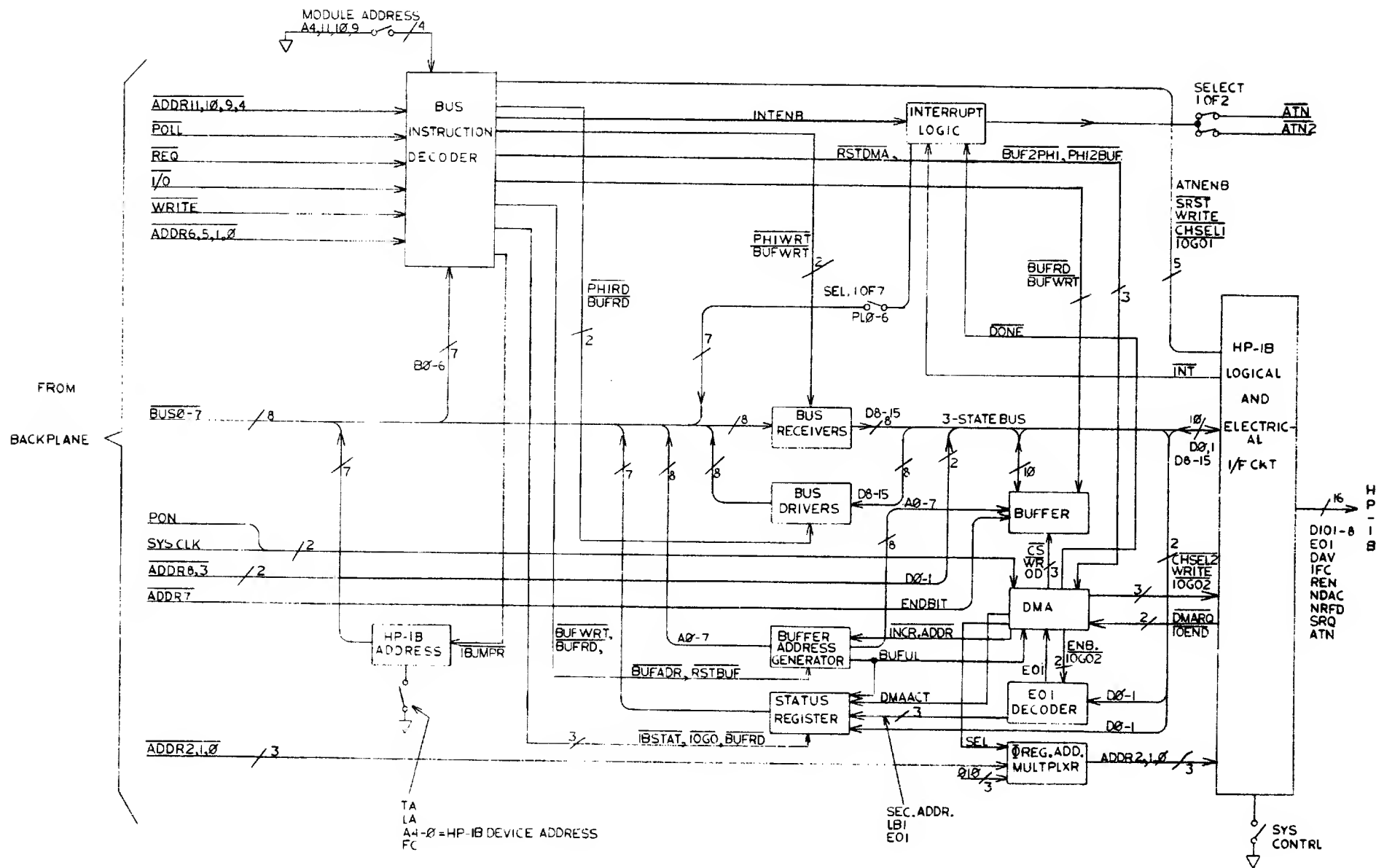


Figure 1  
 HP-IB Interface Module Block Diagram  
 APR-17-79  
 13255-91128

# Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	02640-60128	3	1	HP-18 INTERFACE	28480	02640-60128
C1	0160-4892	6	8	CAPACITOR-FXD 1UF +/-20% 25VDC CER	28480	0160-4892
C2	0160-4892	6		CAPACITOR-FXD 1UF +/-20% 25VDC CER	28480	0160-4892
C3	0160-2055	9	13	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C4	0160-4892	6		CAPACITOR-FXD 1UF +/-20% 25VDC CER	28480	0160-4892
C5	0160-4892	6		CAPACITOR-FXD 1UF +/-20% 25VDC CER	28480	0160-4892
C6	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C7	0160-4892	6		CAPACITOR-FXD 1UF +/-20% 25VDC CER	28480	0160-4892
C8	0160-4892	6		CAPACITOR-FXD 1UF +/-20% 25VDC CER	28480	0160-4892
C9	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C10	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C11	0160-4892	6		CAPACITOR-FXD 1UF +/-20% 25VDC CER	28480	0160-4892
C12	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C13	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C14	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C15	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C16	0160-0393	6	1	CAPACITOR-FXD 39UF +/-10% 10VDC TA	56289	15D0396X901082
C17	0160-1746	5	1	CAPACITOR-FXD 15UF +/-10% 20VDC TA	56289	15D0156X902082
C18	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C20	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C21	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C22	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C23	0160-4892	6		CAPACITOR-FXD 1UF +/-20% 25VDC CER	28480	0160-4892
C24	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
R1	1810-0279	5	4	NETWORK-RES 10-SIP4.7K OHM X 9	01121	210A472
R2	1810-0279	5		NETWORK-RES 10-SIP4.7K OHM X 9	01121	210A472
R4	1810-0279	5		NETWORK-RES 10-SIP4.7K OHM X 9	01121	210A472
R5	0683-3159	5	1	RESISTOR 25.1K 1% .125W P TC=0/+100	24546	C4=1/8-TD-2612-F
R6	0683-1025	9	2	RESISTOR 1K 5% .25W FC TC=400/+600	01121	C81025
R7	1810-0279	5		NETWORK-RES 10-SIP4.7K OHM X 9	01121	210A472
R8	0683-1025	9		RESISTOR 1K 5% .25W FC TC=400/+600	01121	C81025
S1	3101-2094	5	3	SWITCH-RKR DIP-RKR-888Y 8-1A .05A 30VDC	28480	3101-2094
S2	3101-2094	5		SWITCH-RKR DIP-RKR-888Y 8-1A .05A 30VDC	28480	3101-2094
S3	3101-2094	5		SWITCH-RKR DIP-RKR-888Y 8-1A .05A 30VDC	28480	3101-2094
U17	1820-1201	6	5	IC GATE TTL L8 AND QUAD 2-INP	01295	8N74L808N
U18	1820-1470	1	1	IC MUXR/DATA-BEL TTL L8 2-TO-1-LINE QUAD	01295	8N74L8157N
U21	1820-1201	6		IC GATE TTL L8 AND QUAD 2-INP	01295	8N74L808N
U22	1820-1112	8	2	IC FF TTL L8 D-TYPE POS-EDGE-TRIG	01295	8N74L874N
U23	1820-1209	4	1	IC 8FR TTL L8 NAND QUAD 2-INP	01295	8N74L838N
U24	1820-1215	2	1	IC GATE TTL L8 EXCL-OR QUAD 2-INP	01295	8N74L8136N
U25	1820-1917	1	5	IC 8FR TTL L8 LINE DRVR DCTL	01295	8N74L8240N
U27	1820-1917	1		IC 8FR TTL L8 LINE DRVR DCTL	01295	8N74L8240N
U28	1818-0197	2	3	IC NMOS 1K RAM STAT 400-N8 3-8	34335	AM91L118DC
U31	1820-1199	1	5	IC INV TTL L8 HEX 1-INP	01295	8N74L804N
U32	1820-1208	3	4	IC GATE TTL L8 OR QUAD 2-INP	01295	8N74L832N
U33	1820-1281	2	1	IC DCOR TTL L8 2-TO-4-LINE DUAL 2-INP	01295	8N74L8139N
U34	1820-1199	1		IC INV TTL L8 HEX 1-INP	01295	8N74L804N
U35	1820-1917	1		IC 8FR TTL L8 LINE DRVR DCTL	01295	8N74L8240N
U37	1820-1917	1		IC 8FR TTL L8 LINE DRVR DCTL	01295	8N74L8240N
U38	1818-0197	2		IC NMOS 1K RAM STAT 400-N8 3-8	34335	AM91L118DC
U41	1820-1197	9	3	IC GATE TTL L8 NAND QUAD 2-INP	01295	8N74L808N
U42	1820-1201	6		IC GATE TTL L8 AND QUAD 2-INP	01295	8N74L808N
U43	1820-1216	3	1	IC DCOR TTL L8 3-TO-8-LINE 3-INP	01295	8N74L8138N
U44	1820-1208	3		IC GATE TTL L8 OR QUAD 2-INP	01295	8N74L832N
U45	1820-1917	1		IC 8FR TTL L8 LINE DRVR DCTL	01295	8N74L8240N
U46	1820-1201	6		IC GATE TTL L8 AND QUAD 2-INP	01295	8N74L808N
U47	1820-1208	3		IC GATE TTL L8 OR QUAD 2-INP	01295	8N74L832N
U48	1818-0197	2		IC NMOS 1K RAM STAT 400-N8 3-8	34335	AM91L118DC
U49	1820-1430	3	3	IC CNTR TTL L8 SIN SYNCHRD POS-EDGE-TRIG	01295	8N74L8161AN
U51	1820-1568	8	2	IC 8FR TTL L8 8US QUAD	01295	8N74L8125AN
U52	1820-1568	8		IC 8FR TTL L8 8US QUAD	01295	8N74L8125AN
U53	1820-1199	1		IC INV TTL L8 HEX 1-INP	01295	8N74L804N
U54	1820-1201	6		IC GATE TTL L8 AND QUAD 2-INP	01295	8N74L808N
U55	1820-1196	8	1	IC FF TTL L8 D-TYPE POS-EDGE-TRIG COM	01295	8N74L8174N
U56	1820-1197	9		IC GATE TTL L8 NAND QUAD 2-INP	01295	8N74L808N
U57	1820-1112	8		IC FF TTL L8 D-TYPE POS-EDGE-TRIG	01295	8N74L874N
U58	1820-1430	3		IC CNTR TTL L8 SIN SYNCHRD POS-EDGE-TRIG	01295	8N74L8161AN
U59	1820-1217	4	1	IC MUXR/DATA-BEL TTL L8 8-TO-1-LINE	01295	8N74L8151N
U68	1820-1199	1		IC INV TTL L8 HEX 1-INP	01295	8N74L804N
U69	1820-1430	3		IC CNTR TTL L8 SIN SYNCHRD POS-EDGE-TRIG	01295	8N74L8161AN
U111	1820-2058	3	4	IC MISC TTL 8 QUAD	28480	1820-2058
U210	1AA6-6004	0	1	IC, PHI CHIP	28480	1AA6-6004
U211	1820-2058	3		IC MISC TTL 8 QUAD	28480	1820-2058
U311	1820-2058	3		IC MISC TTL 8 QUAD	28480	1820-2058

# Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U410	1820-1197	9		IC GATE TTL LS NANO QUAD 2-INP	01295	8N74L800N
U411	1820-2058	3		IC MISC TTL 3 QUAD	28480	1820-2058
U510	1820-1440	5	1	IC LCM TTL LS QUAD	01295	8N74L8379N
U511	1820-1199	1		IC INV TTL LS HEX 1-INP	01295	8N74L804N
U610	1820-1418	7	1	IC DECOR TTL LS BCD-TO-DEC 4-TO-10-LINE	01295	8N74L842N
U611	1820-1208	3		IC GATE TTL LS OR QUAD 2-INP	01295	8N74L832N
XU26	1200-0539	7		SOCKET-IC 18-CONT OIP-SLOR	28480	1200-0539
XU36	1200-0539	7		SOCKET-IC 18-CONT OIP-SLOR	28480	1200-0539
XU48	1200-0539	7		SOCKET-IC 18-CONT OIP-SLOR	28480	1200-0539
XU210	1200-0847	0	1		28480	1200-0847
				MISCELLANEOUS PARTS		
	0360-0124	3	2	CONNECTOR-89L CONT PIN .04-IN-88C-82 RNO	28480	0360-0124
	0403-0294	0	1	SPACER-PC GUIDE FOR 0.50 IN CO SPCG1 .28	06915	PS-8R
	1200-0844	7	2		28480	1200-0844

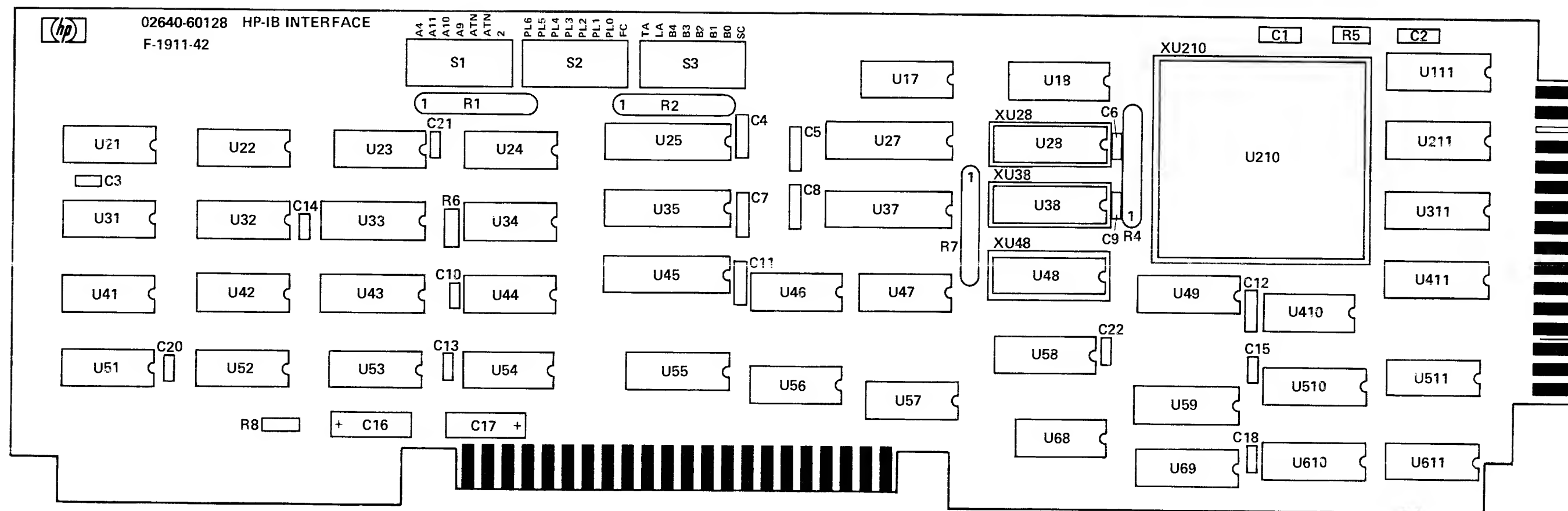


Figure 2  
HP-IB Interface PCA Schematic Diagram  
APR-17-79 13255-91128

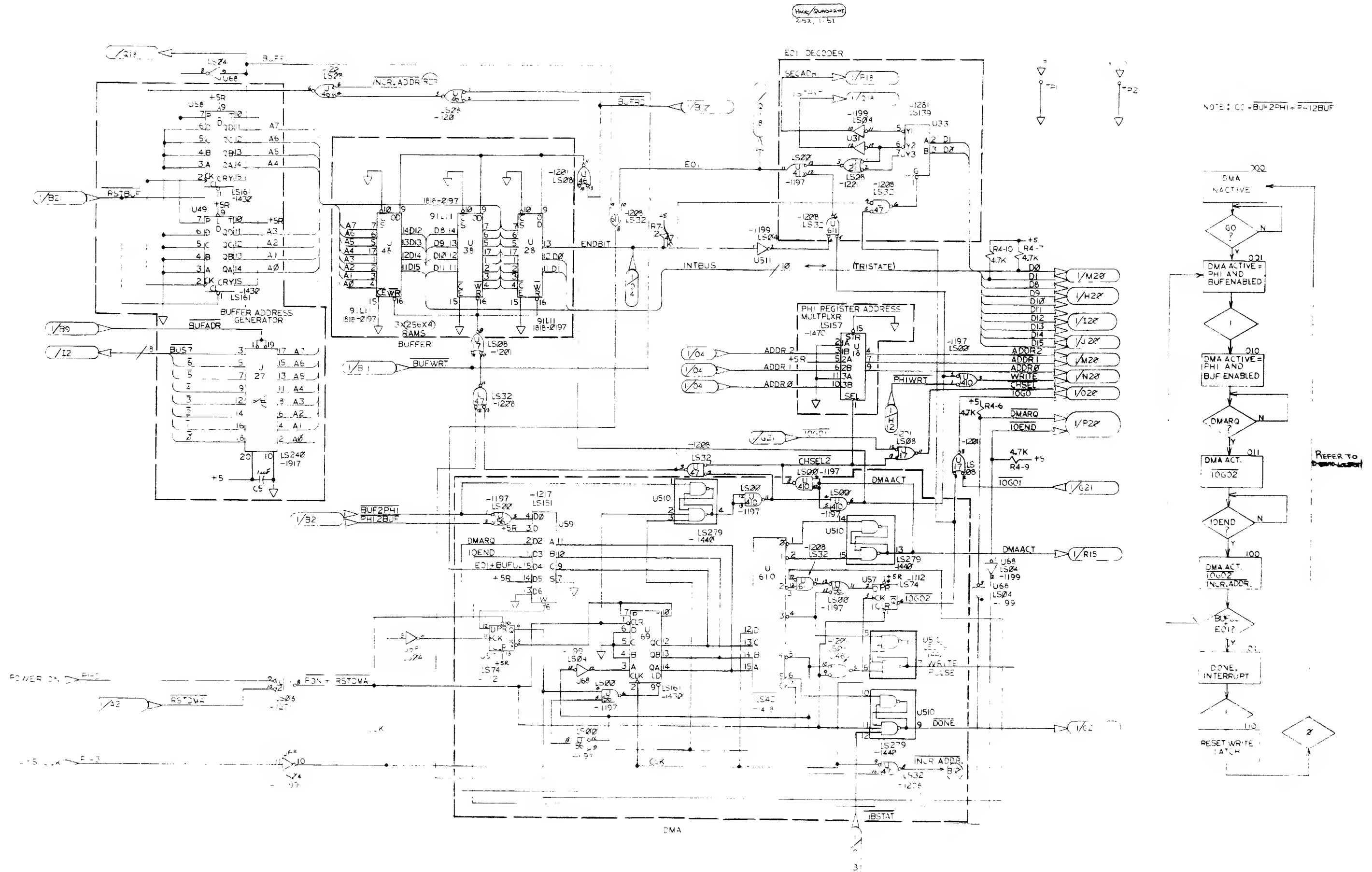
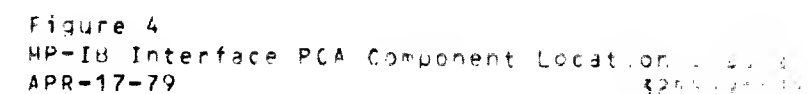


Figure 1





ITEM	LOC	OBJECT CODE	SOURCE STATEMENTS	SAMPLE HP-IB DRIVER - 13255-91128	PAGE 1
2			;	ATTACHMENT 1 - SAMPLE HP-IB DRIVER - 13255-91128	
3			;		
4			;		
5			;		
6			;	NOTICE	
7			;		
8			;	The information contained in this document is subject to change	
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24			;	Copyright c 1976 by HEWLETT-PACKARD COMPANY	
25			;		
26			;		
27			;		
28			;	NOTE: This document is part of the 264XX DATA TERMINAL product	
29			;	series Technical Information Package (HP 13255).	
30			;		

```

=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                                SAMPLE HP-IB DRIVER - 13255-9112B      PAGE  2
=====
32          ;
33          ; DATA TERMINALS DIVISION
34          ; HEWLETT-PACKARD CO.
35          ; (C) 1978
36          ;
37          ; VERSION 1.1 (REV. 2/27/78)
38          ;
39          ; HP-IB ALTERNATE I/O DRIVER CAPABILITIES
40          ;
41          ; THE DRIVER RESIDES AT 24K (DECIMAL) AND REQUIRES 4K OF PROGRAM
42          ; AREA AND USES THE ALTERNATE I/O ENTRY VECTORS. THIS REQUIRES
43          ; THAT A RAM PCA BE STRAPPED FOR THAT START LOCATION.
44          ; IF THE DRIVER IS LOADED VIA THE ASCII LOADER SEQUENCE
45          ; (ESC & C ...) THEN A HARD RESET SHOULD BE PERFORMED
46          ; BEFORE CONTINUING OPERATION.
47          ;
48          ; ALL DATA TRANSFERS TO AND FROM THE HP-IB ARE
49          ; ABORTED IF MORE THAN 1 SECOND IS REQUIRED BEFORE
50          ; THE PHI EITHER ACCEPTS THE NEXT BYTE OR SUPPLIES
51          ; THE NEXT BYTE. TO BYPASS THIS REQUIRES PUTTING
52          ; A 'NOP' AT 'PTPMON' SO THAT THE TIME-OUT COUNTER
53          ; IS NEVER DECREMENTED BY TIMER INTERRUPTS.
54          ;
55          ; THIS DRIVER ASSUMES THAT THE HP-IB PCA (-60128) IS
56          ; STRAPPED AS FOLLOWS:
57          ;
58          ; A4 - CLOSE
59          ; A11 - OPEN
60          ; A10 - CLOSE
61          ; A9 - CLOSE
62          ; ATN - OPEN
63          ; ATN2 - CLOSE
64          ;
65          ; PL6 - CLOSE
66          ; PL5 THRU PLO - OPEN
67          ; FC - CLOSE
68          ;
69          ; TA - CLOSE
70          ; LA - CLOSE
71          ; B4 THRU B0 - CLOSE
72          ; SC - OPEN
73          ;
74          ; * HP-IB is Hewlett-Packard's implementation of
75          ; IEEE standard 488-1975.
76          ;

```

=====				SAMPLE HP-IB DRIVER - 13255-91128		PAGE 3
ITEM	LOC	OBJECT CODE	SOURCE STATEMENTS	=====		
78			;			
79			;			
80			THE FOLLOWING CAPABILITIES ARE AVAILABLE VIA			
81			ESCAPE SEQUENCES AND IN SOME CASES, THE USER CAN			
82			ALSO USE THE GOLD AND GREEN KEY SEQUENCES AND SPECIFY			
83			THE ALTERNATE I/O AS THE DEVICE :			
84			;			
85			INSERT LINE => FROM HP-IB DEVICE			
86			INSERT CHAR => TO HP-IB DEVICE			
87			;			
88			1) SELECT HP-IB TALK ADDRESS (PRIMARY AND SECONDARY)			
89			;			
90			ESC & p 5u 1c <talk address>P			
91			+ => Primary talk address			
92			- => Secondary talk address			
93			;			
94			GREEN, SKIP LINES, <talk address>, INSERT CHAR			
95			;			
96			;			
97			2) SELECT HP-IB LISTEN ADDRESS (PRIMARY AND SECONDARY)			
98			;			
99			ESC & p 5u 2c <listen address>P			
100			+ => Primary listen address			
101			- => Secondary listen address			
102			;			
103			GREEN, FIND FILE, <listen address>, INSERT CHAR			
104			;			
105			;			
106			3) WRITE ONE RECORD FROM I/O BUFFER TO HP-IB DEVICE			
107			SELECTED AS LISTENER			
108			;			
109			ESC & p <user source>s 5d B			
110			;			
111			GOLD, <user source>, INSERT CHAR			
112			;			
113			GREEN, COPY LINE			
114			;			
115			ESC & p W <data> CR LF			
116			;			
117			;			
118			This is valid only when the terminal is in REMOTE			
119			DataCom mode. The data will be input from the DataCom			
120			then written to the HP-IB device.			
			;			

```

=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                                SAMPLE HP-IB DRIVER = 13255-91128      PAGE 4
=====
122      ;
123      ;      4) READ ONE RECORD TO I/O BUFFER FROM HP-IB DEVICE
124      ;      SELECTED AS TALKER
125      ;
126      ;      ESC & p 5s <user destination>d B
127      ;
128      ;      GOLD, INSERT LINE, <user destination>
129      ;
130      ;      GREEN, COPY LINE
131      ;
132      ;      ESC & p R <data> CR LF
133      ;
134      ;      This is valid only when the terminal is in REMOTE
135      ;      DataCom mode. The data will be read from the HP-IB
136      ;      device then output to DataCom.
137      ;
138      ;      5) INITIALIZE HP-IB PCA
139      ;
140      ;      ESC & p 5u 0C
141      ;
142      ;      GREEN, REWIND, INSERT CHAR
143      ;
144      ;
145      ;      6) SELF-TEST OF HP-IB PCA
146      ;
147      ;      ESC & p 5u 5C
148      ;
149      ;      GREEN, MARK FILE, INSERT CHAR
150      ;
151      ;
152      ;      7) SELECT HP-IB CONTROL FUNCTIONS
153      ;
154      ;      A) MONITOR MODE OF HP-IB COMMAND AND DATA TRANSFERS
155      ;
156      ;      ESC & p 5u 3c 0P (Turn on monitor mode)
157      ;
158      ;      ESC & p 5u 3c 1P (Turn off monitor mode)
159      ;
160      ;      No GREEN sequence available.

```

```

=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                                SAMPLE HP-IB DRIVER - 13255-91128      PAGE 5
=====
162      ;
163      ;      B) SELECT NON-CONTROLLER MODE OPERATIONS
164      ;      when the 'SC' switch is closed, this will allow
165      ;      data transfers to and from the HP-IB to occur
166      ;      without generating a non-controller error.
167      ;      The operation must be initiated by an external
168      ;      request, not by the user at the keyboard. The
169      ;      power-on default is determined by 'LA' switch.
170      ;      When it is opened and the 'SC' switch is closed,
171      ;      then non-controller mode is automatically enabled.
172      ;      This allows another HP-IB controller to control
173      ;      the terminal and its associated I/O devices thru
174      ;      the HP-IB interface.
175      ;
176      ;      ESC & p 5u 3c 2P (Enable non-controller mode)
177      ;
178      ;      ESC & p 5u 3c 3P (Disable non-controller mode)
179      ;
180      ;      No GREEN sequence available.
181      ;
182      ;      C) REN CONTROL
183      ;
184      ;      ESC & p 5u 3c 4P (Turn on HP-IB REN line)
185      ;
186      ;      ESC & p 5u 3c 5P (Turn off HP-IB kEN line)
187      ;
188      ;      No GREEN sequence available.
189      ;
190      ;      D) IFC CONTROL
191      ;
192      ;      ESC & p 5u 3c 6P (Turn on HP-IB IFC line)
193      ;
194      ;      ESC & p 5u 3c 7P (Turn off HP-IB IFC line)
195      ;
196      ;      E) SRQ CONTROL
197      ;
198      ;      ESC & p 5u 3c 8P (Turn on HP-IB SRQ line)
199      ;
200      ;      ESC & p 5u 3c 9P (Turn off HP-IB SRQ line)
201      ;
202      ;      F) PARALLEL POLL CONTROL
203      ;
204      ;      ESC & p 5u 3c 10P (Turn on poll bit)
205      ;
206      ;      ESC & p 5u 3c 11P (Turn off poll bit)

```

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=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                                SAMPLE HP-IB DRIVER - 13255-91128      PAGE   6
=====
208      ;
209      ;          G) EXTENDED STATUS REQUEST
210      ;
211      ;          ESC & p 5u 3c 12P (General status)
212      ;
213      ;          ESC & p 5u 3c 13P (SRQ status)
214      ;
215      ;          ESC & p 5u 3c 14P (Parallel poll status)
216      ;
217      ;          ESC & p 5u 3c 15P (Reserved)
218      ;
219      ;      8) SET PARALLEL POLL MASK
220      ;      This provides a bit mask that qualifies the parallel
221      ;      poll response before returning status.
222      ;      Each address is OR'ed with any previous addresses
223      ;      specified. A value of 8 or greater clears this mask.
224      ;
225      ;          ESC & p 5u 6c <HP-IB address>P
226      ;
227      ;      9) SET SRQ ADDRESS TABLE
228      ;      This is the list of HP-IB addresses that will be serial
229      ;      polled when SRQ is true on the HP-IB.
230      ;      Each address is OR'ed with any previous addresses
231      ;      specified. A value of 31 or greater clears the list.
232      ;
233      ;          ESC & p 5u 7c <HP-IB address>P
234      ;
235      ;      10) OUTPUT DATA BYTE WITH EOI TRUE
236      ;      Assumes proper HP-IB addressing has been performed
237      ;      beforehand.
238      ;
239      ;          ESC & p 5u 8c <data>P
240      ;
241      ;      11) OUTPUT DATA BYTE
242      ;      Assumes HP-IB addressing has been done beforehand.
243      ;
244      ;          ESC & p 5u 9c <data>P
245      ;
246      ;      12) OUTPUT HP-IB COMMANDS
247      ;
248      ;          ESC & p 5u 10c <byte to be written> P
249      ;
250      ;      No GREEN sequence available.
251      ;

```

```

=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                                SAMPLE HP-IB DRIVER - 13255-91128      PAGE 7
=====
253      ;
254      ;                                HP-IB PCA (02640-60128)
255      ;
256      ;
257      ;      +-----+      +-----+      +-----+
258      ;      | General |<--->| Burst  |<--->| PHI   |
259      ;      | Interface|      | Transfer|      | Interface|<-->HP-IB
260      ;      +-->| Registers| +-->| Registers| +-->| Registers|
261      ;      \ +-----+      ! +-----+      / +-----+
262      ;      \ | IBSTAT |      ! | IBBFRD |      / | PHIRG0 |
263      ;      \ | STAT   |      ! | BUFRD  |      / | LPHIRO |
264      ;      \ | IBCNTL |      ! | IBBFWR |      / | PHIRG1 |
265      ;      \ | CNTL   |      ! | BUFWR  |      / | LPHIR1 |
266      ;      \ | IBJMPR |      ! | IBBFAD |      / |      :  |
267      ;      \ | READJP |      ! | BUFADR |      / |      :  |
268      ;      \ +-----+      ! +-----+      / |      :  |
269      ;      \      v      / |      :  |
270      ;      +----->+<-----+      |      :  |
271      ;      ^      | PHIRG7 |
272      ;      +-----+      | LPHIR7 |
273      ;      | Module |
274      ;      | Select |
275      ;      +-----+
276      ;      v
277      ;      -----+----- 2645 Backplane -----+-----
278      ;

```



```

=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                                SAMPLE HP-IB DRIVER - 13255-91128      PAGE 8
=====
280          ;
281          ; ALTERNATE I/O HP-IB DRIVER
282          ;
283          ;*****
284          ; MAIN CODE VARIABLES USED BY DRIVER *
285          ;*****
286      FFC0      CURROW EQU 177700Q      ;CURSOR ROW
287      FFC1      CURCOL EQU 177701Q      ;CURSOR COLUMN
288      8700      IOCRL EQU 103400Q      ;DMA CURSOR COLUMN
289      8720      IOCRRW EQU 103440Q      ;DMA CURSOR ROW
290      8380      IOKBCO EQU 101600Q      ;KEYBOARD CONTROL
291      0002      RSTON EQU 2Q            ;RESET ENABLE
292          ;
293      FFD8      IOCTYP EQU 177730Q      ;TYPE OF CONTROL CALL
294      FFD5      IOCCNF EQU 177725Q      ;CONTROL CALL PARAMETER
295      FF4F      IOCERR EQU 177517Q      ;ERROR FLAG: MAY BE S,F,OR U
296      FFDC      IOPSGN EQU 177734Q      ;SIGN VALUE OF PARAMETER
297      0053      S      EQU 123Q
298      0046      F      EQU 106Q
299      0055      U      EQU 125Q
300      FF4B      IOSTA3 EQU 177513Q      ;DEVICE STATUS 3
301      FF4A      IOSTA2 EQU IOSTA3-1      ;DEVICE STATUS 2
302      FF49      IOSTA1 EQU IOSTA2-1      ;DEVICE STATUS 1
303      FFF1      MSGPT1 EQU 177761Q      ;POINTER TO ERROR MESSAGE
304      FFEF      MSGPT2 EQU MSGPT1-2      ; " " " "
305      0082      INVRS EQU 202Q          ;INVERSE VIDEO FOR ERROR MSG
306      008A      HALFBR EQU 212Q          ;HALF BRIGHT, INVERSE VIDEO
307      00CE      EOP EQU 316Q            ;END OF MESSAGE
308      9168      SCNVEC EQU 110550Q
309      0064      TIMEOUT EQU 100          ;TIME OUT VALUE= 1 SEC
310      000F      XFRCNT EQU 17Q          ;COUNTER FOR FIFO CHECKOUT
311      FF00      BASE2 EQU 177400Q      ;START BASE OF VARIABLES
312      001B      ESC EQU 33Q            ;ESCAPE CHARACTER
313          ;*****
314          ; I/O BUFFERS *
315          ;*****
316      FC00      IOBUF1 EQU 176000Q
317      FF3A      B1STAT EQU 177472Q      ;STATUS -
318      FF39      B1TYPE EQU B1STAT-1      ;TYPE: -1 => DATA RECORD
319          ;                                ; 0 => END OF FILE
320          ;                                ; 1 => END OF DATA
321      FF38      B1LEN EQU B1TYPE-1
322          ;
323      FD00      IOBUF2 EQU 176400Q
324      FF37      B2STAT EQU 177467Q
325      FF36      B2TYPE EQU B2STAT-1
326      FF35      B2LEN EQU B2TYPE-1
327          ;
328      0010      ALTIO EQU 20Q            ;BIT IN STATUS CLAIMS BUFFER
329          ;

```

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=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                                SAMPLE HP-IB DRIVER - 13255-91128      PAGE  9
=====
331          ;
332          ;*****
333          ; ENTRIES TO OTHER MODULES *
334          ;*****
335      0040      DSPMSG EQU 100Q      ;DISPLAY MESSAGE
336      0082      CHINT EQU 202Q      ;MAIN: CHARACTER INTERPRET
337      4805      ZGETKY EQU 44005Q   ;KEYBOARD: GET KEY
338      00C3      JMP EQU 303Q      ;8080 JMP INSTRUCTION
339          ;
340          ; LOCAL VARIABLE ALLOCATION (FAST RAM)
341          ;
342      9100      BASE EQU 110400Q
343      9180      START EQU 110600Q
344      917F      XREG0 EQU START-1      ;CURRENT VALUES OF PHI REGISTERS
345      917E      XREG1 EQU XREG0-1
346      917D      XREG2 EQU XREG1-1
347      917C      XREG3 EQU XREG2-1
348      917B      XREG4 EQU XREG3-1
349      917A      ADDRST EQU XREG4-1      ;CURRENT JUMPER VALUES
350      9179      XTIMER EQU ADDRST-1      ;TIME OUT COUNTER
351      9178      ADRLIS EQU XTIMER-1      ;LISTEN ADDR
352      9177      LISSEC EQU ADRLIS-1      ;LISTEN SECONDARY ADDR
353      9176      ADRTLK EQU LISSEC-1      ;TALKER ADDRESS
354      9175      TLKSEC EQU ADRTLK-1      ;TALK SECONDARY ADDRESS
355      9174      IBFLGS EQU TLKSEC-1      ;SPECIAL FLAGS
356      0001      OKTOXM EQU 1Q      ;OK TO TRANSMIT
357      0002      NCM EQU 2Q      ;NON-CONTROLLER MODE
358      0004      PPRESP EQU 4Q      ;PARALLEL POLL RESPONSE
359      9173      CNTLWD EQU IBFLGS-1      ;CURRENT VALUE FOR 'IBCNTL'
360      9172      IBADR2 EQU CNTLWD-1      ;HP-IB ADDRESS
361      9171      SECNDY EQU IBADR2-1      ;SECONDARY ADDRESS
362      916F      BFADR2 EQU SECNDY-2      ;BUFFER ADDRESS START
363      916E      BFLEN2 EQU BFADR2-1      ;NO. OF CHARS
364      916D      FLAGS2 EQU BFLEN2-1      ;OPTIONS FOR HP-IB DVRS
365          ;
366      0001      LFDET EQU 1Q      ; END HP-IB XFER ON 'LF' CHAR
367      0080      DMA EQU 200Q      ;USE DMA FOR DATA TRANSFER
=====

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=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                                SAMPLE HP-IB DRIVER - 13255-91128      PAGE 10
=====
369          ;
370          ; LOCAL VARIABLE ALLOCATION (SLOW RAM)
371          ;
372          ;*****
373      FE68      SLOW      EQU      177150Q
374      FE64      SRQTBLE EQU      SLOW-4      ;SRQ TABLE VALUES
375      FE63      PPBYTE   EQU      SRQTBLE-1    ;PARALLEL POLL MASK
376      FE62      SRQADR   EQU      PPBYTE-1    ;LAST SRQ ADDR THAT ANSWERED
377      FE61      PPADR    EQU      SRQADR-1    ;LAST STATE OF PARALLEL POLL
378      FE60      STYPE    EQU      PPAOR-1     ;STATUS TYPE TO BE RETURNED
379      FE5F      SRQSTA   EQU      STYPE-1     ;SRQ STATUS RETURNED BY DEVICE
380      FE5E      MASK     EQU      SRQSTA-1    ;HP-IB PARALLEL POLL MASK
381      FE5D      STRT2    EQU      MASK-1      ;TYPE OF ERROR RETURN
382      FE5C      FLGSAV   EQU      STRT2-1     ;TEMP STORAGE
383      FE5B      FLGSV1   EQU      FLGSAV-1    ;TEMP STORAGE
384      FE59      HIBVEC   EQU      FLGSV1-2    ;INTERRUPT VECTOR
385      FE58      HIBCNT   EQU      HIBVEC-1    ;TEST COUNTER
386      FE57      HIBERR   EQU      HIBCNT-1    ;TEST ERROR STATUS
387      FE56      HIBSTT   EQU      HIBERR-1    ;TEST INTERRUPT STATUS
388      0001      ERRINT   EQU      1Q          ; ERROR OCCURRED
389      0002      FIN      EQU      2Q          ; TEST COMPLETED
390      0004      IDLEERR  EQU      4Q          ; ILLEGAL INTERRUPT
391      FE55      TESTNO   EQU      HIBSTT-1    ;CURRENT TEST NUMBER
392      FE54      ERRNO    EQU      TESTNO-1    ;ERROR NUMBER

```

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=====
ITEM    LOC    OBJECT CODE  SOURCE STATEMENTS                                SAMPLE HP-IB DRIVER - 13255-91128    PAGE 11
=====
394          ;
395          ; HP-IB FUNCTION SELECT STROBES
396          ;
397    0020    BUFRD EQU 40Q      ;READ DATA FROM BUFFER
398    0020    BUFVRT EQU 40Q     ;WRITE DATA TO BUFFER
399    0041    BUFADR EQU 101Q    ;READ BUFFER ADDR REG
400          ;
401    0010    EOIBIT EQU 20Q     ;EOI STATUS BITS
402    0003    EOITYP EQU 3Q      ;EOI STATUS BITS
403    0080    ENDBIT EQU 200Q    ;SIGNAL LAST BYTE TO DMA
404          ;
405    0042    READJP EQU 102Q    ;READ JUMPERS
406    0000    PHIREG EQU 00
407    0040    STAT EQU 100Q     ;STATUS
408    0040    CNTL EQU 100Q     ;CONTROL
409          ;
410          ; HP-IB MODULE ADDRESSES
411          ;
412    0008    IB EQU 100         ;MODULE 4
413    0088    HPIB EQU 200Q+IB
414    8800    HPIBAD EQU HPIB*256
415    8800    IBREG EQU HPIBAD+PHIREG ;BASE ADDR OF PHI REG
416    8842    IBJMPR EQU HPIBAD+READJP ;JUMPER ADDR
417    8840    IBSTAT EQU HPIBAD+STAT ;STATUS ADDR
418    8840    IBCNTL EQU IBSTAT ;CONTROL ADDR
419    8820    IBBFRD EQU HPIBAD+BUFRD ;READ BUFFER DATA
420    8820    IBBFWR EQU HPIBAD+BUFVRT ;WRITE BUFFER DATA
421    8841    IBBFAD EQU HPIBAD+BUFADR ;READ BUFFER ADDR REG
422          ;
423    8800    PHIRG0 EQU IBREG+0 ;PHI REG 0
424    8801    PHIRG1 EQU IBREG+1 ; "
425    8802    PHIRG2 EQU IBREG+2 ; "
426    8803    PHIRG3 EQU IBREG+3 ; "
427    8804    PHIRG4 EQU IBREG+4 ; "
428    8805    PHIRG5 EQU IBREG+5 ; "
429    8806    PHIRG6 EQU IBREG+6 ; "
430    8807    PHIRG7 EQU IBREG+7 ;PHI REG 7

```

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=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                                SAMPLE HP-IB DRIVER - 13255-91128      PAGE 12
=====
432              ;
433              ; HP-IB TEST
434              ;
435      0055      D125      EQU      125Q
436      00AA      D252      EQU      252Q
437      0000      LPHIR0 EQU      PHIRG0-IBREG
438      0001      LPHIR1 EQU      LPHIR0+1
439      0002      LPHIR2 EQU      LPHIR0+2
440      0003      LPHIR3 EQU      LPHIR0+3
441      0004      LPHIR4 EQU      LPHIR0+4
442      0005      LPHIR5 EQU      LPHIR0+5
443      0006      LPHIR6 EQU      LPHIR0+6
444      0007      LPHIR7 EQU      LPHIR0+7
445      000F      TSTCHR EQU      17Q
446      00FF      TSTLST EQU      377Q
447      0080      ENDTBL EQU      200Q
448              ;
449      0030      ZERO      EQU      60Q
450      0031      ONE       EQU      61Q
451      0032      TWO       EQU      62Q
452      0033      THREE     EQU      63Q
453      0034      FOUR      EQU      64Q
454      0035      FIVE      EQU      65Q
455      0036      SIX       EQU      66Q
456      0037      SEVEN     EQU      67Q
457      0038      EIGHT     EQU      70Q
458      0039      NINE      EQU      71Q
459      003A      TEN       EQU      72Q
460      003B      ELEVEN    EQU      73Q
461      003C      TWELVE    EQU      74Q
462      003D      THRTEEN   EQU      75Q
463      003E      FORTEN    EQU      76Q
464      003F      FIFTEN    EQU      77Q
465      0040      SIXTEN    EQU      100Q
466      0041      SEVTEN    EQU      101Q
=====

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=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                                SAMPLE HP-IB DRIVER - 13255-91128      PAGE 13
=====
468      ;
469      ; PHI REGISTER 0
470      ;
471      0001      DEVCLR EQU 1Q          ;DEVICE CLEAR
472      0002      OTFEMP EQU 2Q          ;OUT FIFO EMPTY
473      0004      INFIFO EQU 4Q          ;IN-FIFO NOT EMPTY
474      0008      OTFIFO EQU 10Q         ;OUT-FIFO NOT FULL
475      0010      SRQIN EQU 20Q          ;SERVICE REQUEST RESPONSE
476      0020      PPIN EQU 40Q           ;PARALLEL POLL RESPONSE
477      0040      PABORT EQU 100Q        ;PROCESSOR ABORT
478      0080      STCHNG EQU 200Q        ;STATUS CHANGE
479      ;
480      ; PHI REGISTER 3 -
481      ;
482      0001      FREEZE EQU 1Q          ;OUT FIFO FREEZE
483      0002      P3LSTN EQU 2Q          ;PHI IS CURRENTLY LISTENER
484      0004      P3TALK EQU 4Q          ;PHI IS CURRENTLY TALKER
485      0008      SYSCTL EQU 10Q         ;SYSTEM CONTROLLER
486      0010      CIC EQU 20Q           ;CONTROLLER IN CHARGE
487      0020      REMOTE EQU 40Q         ;REMOTE
488      ;
489      ; INPUT D0,D1 FOR REG. 0,1,2 VIA PHI REG 3
490      ; (8 BIT PROCESSOR MODE)
491      ;
492      0040      PARERR EQU 100Q        ;PARITY ERROR
493      0000      IDATA EQU 0Q           ;DATA BYTE
494      00C0      IEQI EQU 300Q          ;DATA BYTE WITH EOI
495      0080      IEND EQU 200Q          ;DATA BYTE SATISFIES
496      ; COUNT REQUEST
497      0040      ISEC EQU 100Q          ;SECONDARY COMMAND
498      ;
499      ; PHI REGISTER 4 - OUTPUT - D0,D1
500      ;
501      0001      INITFF EQU 1Q          ;INITIALIZE OUT FIFO
502      0002      DNASEL EQU 2Q          ;SELECT DMA XFER DIRECTION
503      0004      SRQOUT EQU 4Q          ;SERVICE REQUEST
504      0008      PPOUT EQU 10Q          ;PARALLEL POLL
505      0010      IFC EQU 20Q            ;INTERFACE CLEAR
506      0020      REN EQU 40Q            ;REMOTE ENABLE
507      0040      PFRZ EQU 100Q          ;PARITY FREEZE
508      0080      P8BIT EQU 200Q         ;8 BIT PROCESSOR MODE
509      ;
510      ; OUTPUT D0,D1 FOR REG. 0,1,2 VIA PHI REG 4
511      ; (8 BIT PROCESSOR MODE)
512      ;
513      0000      ODATA EQU 0Q           ;DATA BYTE
514      0080      OEOI EQU 200Q          ;EOI BYTE
515      0040      OIFCOM EQU 100Q        ;INTERFACE COMMAND
516      00C0      OREC EQU 300Q          ;RECEIVE DATA
517      00C0      OHNDS EQU 300Q         ;HANDSHAKE DATA

```

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=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                                SAMPLE HP-IB DRIVER - 13255-91128      PAGE  14
=====
519          ;
520          ; PHI REGISTER 5 CONTROL BITS
521          ;
522      0020      LA      EQU   40Q      ;LISTEN ALWAYS
523      0040      TA      EQU  100Q      ;TALK ALWAYS
524      0080      ONLINE EQU  200Q      ;ON-LINE STATUS
525          ;
526      001E      HPTERM EQU  36Q      ;2645 TERMINAL
527      001F      UNLSAD EQU  37Q      ;UNLISTEN ADDRESS
528      0080      NOSEC  EQU  200Q      ;NO SECONDARY
529          ;
530          ; HP-IB PCA CONTROL BITS (IBCNTRL)
531          ;
532      0001      PON     EQU   1Q      ;POWER-ON STROBE
533      0002      ATNENB EQU   2Q      ;HP-IQ ATTENTION ENABLE
534      0004      BF2PHI EQU   4Q      ;INITIATE BUFFER TO PHI XFER
535      0008      PHI2BF EQU  10Q      ;INITIATE PHI TO BUFFER XFER
536      0010      RSTBUF EQU  20Q      ;RESET BUFFER ADDR REG.
537      0020      INTENB EQU  40Q      ;ENABLE BUFFER-TYPE INTERRUPT
538      0040      RSTDMA EQU 100Q      ;DMA ABORT
539          ;
540          ; HP-IB PCA STATUS BITS (IBSTAT)
541          ;
542      0001      D1      EQU   1Q      ;D1 DATA BIT FROM PHI,RAM
543      0002      D0      EQU   2Q      ;D0 DATA BIT FROM PHI,RAM
544      0004      SECDAT EQU   4Q      ;SECONDARY DATA BYTE
545      0008      LSTBYT EQU  10Q      ;LAST DATA BYTE, TYPE 1
546      0010      EOI2TT EQU  20Q      ;EOI OCCURRED
547      0020      BUFFUL EQU  40Q      ;BUFFER IS FULL
548      0040      DMAACT EQU 100Q      ;DMA IS ACTIVE
549      0003      IEOI2  EQU D0+D1      ;EOI IS TRUE FOR THIS BYTE
550      0001      ISEC2  EQU  D1      ;THIS IS A SECONDARY ADDR
551          ;
552          ; HP-IB PCA JUMPERS (IBJMPR)
553          ;
554      001F      ADDR    EQU  370      ;ADDRESS OF TERMINAL WHEN NOT CONTROLLER
555      0020      LASW    EQU  400      ;LISTEN ALWAYS SWITCH
556      0040      TASW    EQU 1000      ;TALK ALWAYS SWITCH
557      0080      FCSW    EQU 2000      ;FIRMWARE CONTROL SWITCH
=====

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=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                                SAMPLE HP-IB DRIVER - 13255-91128      PAGE 15
=====
559          ;
560          ; D0,D1 WHEN WRITING TO REGISTER 0,1,2
561          ; (ADDRESS BITS 4,3)
562          ;
563      0008      PARER2 EQU 100          ;PARITY ERROR
564      0010      PHIINT EQU 200         ;PHI INTERRUPT ENABLE
565          ;
566      0000      DATA2 EQU 0Q          ;DATA BYTE BEING WRITTEN (ATN FALSE)
567      0010      EQI2 EQU 20Q          ;EQI BYTE BEING WRITTEN (ATN FALSE)
568      0008      IFCOM2 EQU 10Q        ;INTERFACE COMMAND BEING WRITTEN (ATN TRUE)
569      0018      REC2 EQU 30Q          ;RECEIVE DATA COUNT
570      0018      HNDS2 EQU 30Q         ;HANDSHAKE DATA BETWEEN DEVICES
571          ;
572          ; HP-IB INTERFACE COMMANDS
573          ;
574      0020      LISBIT EQU 40Q         ;LISTEN ADDRESS
575      0040      TLKBIT EQU 100Q       ;TALK ADDRESS
576      0060      SECBIT EQU 140Q      ;SECONDARY ADDRESS
577      0020      SECTLK EQU 40Q        ;BIT FOR SEC COMM T/L
578          ;
579      000A      LF EQU 12Q            ;LINE FEED
580          ;
581          ; HP-IB ADDRESSED COMMAND GROUP
582          ;
583      0001      GTL EQU 1Q            ;GO TO LOCAL
584      0004      SDC EQU 4Q            ;SELECTED DEVICE CLEAR
585      0008      GET EQU 10Q          ;GRDUP EXECUTE TRIGGER
586      0009      TCT EQU 11Q          ;TAKE CONTROL
587          ;
588          ; HP-IB UNIVERSAL COMMAND GROUP
589          ;
590      0011      LLO EQU 21Q           ;LOCAL LOCKOUT
591      0014      DCL EQU 24Q           ;DEVICE CLEAR
592      0018      SPE EQU 30Q           ;SERIAL POLL ENABLE
593      0019      SPD EQU 31Q           ;SERIAL POLL DISABLE
594          ;
595      0040      SRMSK EQU 100Q        ;AFFIRMATIVE SRQ RESPONSE
596      00FF      ONES EQU 377Q        ;ALL BITS ON
597      001E      TERMID EQU 30         ;HP-IB CONTROLLER ADDRESS
598      001F      ADRMSK EQU 37Q       ;ADDRESS BIT MASK FOR JUMPERS
599      0014      GETCTL EQU 20        ;IFC SHOULD LAST THIS LONG
600      0020      MAXADR EQU 32        ;MAXIMUM HP-IB ADDRESS VALUE
601      0001      SECADR EQU 1         ;D0,D1 BITS FOR SECONDARY ADDRESS
602      0000      DATA EQU 0          ;D0,D1 BITS FOR DATA
603      0040      DMAFL EQU 100Q       ;DMA FAILURE
604      0041      TIMERR EQU 101Q      ;TIME OUT ERROR
605      0042      NOCIC EQU 102Q       ;NOT CONTROLLER IN CHARGE
606      0043      BADADR EQU 103Q      ;CALLER SUPPLIED ILLEGAL HP-IB ADDRESS
607      0044      NOSRQ EQU 104Q       ;SRQ NOT ASSERTED ON HP-IB
608      0045      NSYS EQU 105Q        ;NOT SYSTEM CONTROLLER

```



```

=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                                SAMPLE HP-IB DRIVER = 13255-91128      PAGE 16
=====
610      0000                                ORG 60000Q
611      6000                                ALSTRT EQU $ ;STARTING ADDRESS
612      6000      50                                DEF 120Q ;CODE PRESENT, VERSION 0
613      6001      60                                DEF ALSTRT/256 ;CHECK FOR CORRECT LOCATION
614                                          ;
615                                          ; ENTRY VECTORS
616                                          ;
617      6002      C3 59 62                                JMP PTPINI ;INITIALIZATION
618      6005      C3 D8 62                                JMP PTPIN2 ;INITIALIZATION CONTINUATOR
619      6008      C3 25 60                                JMP INTPTP ;INTERRUPT
620      600B      C3 A1 6C                                JMP PTPMON ;MONITOR
621      600E      C3 9B 6A                                JMP PTP2BF ;INPUT RECORD FROM HP-IB
622      6011      C3 35 6A                                JMP BF2PTP ;OUTPUT RECORD TO HP-IB
623      6014      C3 DA 62                                JMP PTPCTR ;CONTROL
624      6017      C3 AA 61                                JMP STAPTP ;STATUS (NONE - JUST RET)
625      601A      20 4F 4E                                DEF ' ON HP-IB ',0

```

```

=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                                SAMPLE HP-1B DRIVER - 13255-91128      PAGE 17
=====
627      ;
628      ;
629      ;   INTERRUPT ROUTINES FOR SELF-TEST
630      ;
631      ;
632      6025      INTPTP EQU $
633      6025      2A 59 FE      LHLD HIBVEC      ;GET CURRENT INT ROUTINE
634      6028      E9              PCHL
635      ;
636      ;   WRTINT - WRITE DATA BYTES TO PHI DURING
637      ;   INTERRUPT PROCESSING...
638      ;
639      6029      WRTINT EQU $
640      6029      C5              PUSH B
641      602A      26 88          MVI H,HP1B      ;BE SURE IT IS THE RIGHT
642      602C      2E 00          MVI L,LPHIRO
643      602E      7E              MOV A,M
644      602F      E6 08          ANI OTFIFO      ; INTERRUPT
645      6031      CA 49 61      JZ   ERR103
646      6034      3A 58 FE      LDA HIBCNT      ;GET THE COUNTER
647      6037      4F              MOV C,A
648      6038      B7              ORA A          ;LAST ONE?
649      6039      CA 48 60      JZ   WRI010      ;YES
650      603C      2E 02          MVI L,LPHIR2+DATA2 ;NO, WRITE DATA BYTES
651      603E      77              MOV M,A
652      603F      3D              DCR A          ;UPDATE COUNTER
653      6040      WRI005 EQU $
654      6040      32 58 FE      STA HIBCNT
655      6043      C1              POP B
656      6044      E1              POP H
657      6045      F1              POP PSW
658      6046      FB              EI
659      6047      C9              RET
660      ;
661      6048      WRI010 EQU $
662      6048      2E 12          MVI L,LPHIR2+E012 ;WRITE LAST BYTE
663      604A      77              MOV M,A
664      604B      2E 00          MVI L,LPHIRO      ;STILL NEED MORE DATA?
665      604D      7E              MOV A,M
666      604E      E6 08          ANI OTFIFO
667      6050      C2 4E 61      JNZ ERR104      ;YES, ERROR
668      6053      WRI020 EQU $
669      6053      21 21 61      LXI H,IDLE      ;RESET INTERRUPT VECTOR
670      6056      22 59 FE      SHLD HIBVEC
671      6059      3A 56 FE      LDA HIBSTI      ;SET SUCCESSFUL FINISH
672      605C      E6 FC          ANI ONES-ERRINT-FIN
673      605E      F6 02          ORI FIN
674      6060      32 56 FE      STA HIBSTI
675      6063      C1              POP B
676      6064      E1              POP H
677      6065      F1              POP PSW
678      6066      FB              EI
679      6067      C9              RET

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681      ;
682      ; RDINT - READ DATA BYTES UNDER INTERRUPT
683      ;
684      6068      RDINT EQU $
685      6068      C5      PUSH B
686      6069      26 88      MVI H,HPIB      ;RIGHT INTERRUPT?
687      606B      2E 00      MVI L,LPHIRO
688      606D      7E          MOV A,M
689      606E      E6 04      ANI INFIFO
690      6070      CA 49 61      JZ   ERR103      ;NO
691      6073      2E 02      MVI L,LPHIR2      ;YES, GET BYTE
692      6075      7E          MOV A,M
693      6076      47          MOV B,A
694      6077      2E 40      MVI L,STAT      ;DATA BYTE?
695      6079      7E          MOV A,M
696      607A      E6 03      ANI D0+D1
697      607C      C2 8D 60      JNZ RD010      ;NO
698      607F      3A 58 FE      LDA HIBCNT      ;YES, CORRECT VALUE?
699      6082      B8          CMP B
700      6083      C2 4E 61      JNZ ERR104      ;NO
701      6086      3D          DCR A      ;YES, UNDERFLOW?
702      6087      FA 53 61      JM   ERR105      ;YES
703      608A      C3 40 60      JMP WRI005      ;NO, KEEP GOING
704      ;
705      608D      RD010 EQU $
706      608D      FE 03      CPI IEQ12      ;EOI BYTE?
707      608F      78          MOV A,B
708      6090      C2 58 61      JNZ ERR106      ;NO, ERROR
709      6093      87          ORA A
710      6094      C2 5D 61      JNZ ERR107      ;NO, EOI AT WRONG BYTE
711      6097      2E 00      MVI L,LPHIRO      ;ANY MORE DATA?
712      6099      7E          MOV A,M
713      609A      E6 04      ANI INFIFO
714      609C      C2 62 61      JNZ ERR108      ;YES, ERROR
715      ;
716      609F      C3 53 60      JMP WRI020

```

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=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                                SAMPLE HP-IB DRIVER - 13255-91128      PAGE 19
=====
718                                     ;
719                                     ; WRDMA - DMA INTERRUPT WRITE ROUTINE
720                                     ;
721      60A2                                     WRDMA EQU $
722      60A2      C5                                     PUSH B
723      60A3      26 88                                     MVI H,HPIB      ;CHECK FOR COMPLETION STATUS
724      60A5      2E 40                                     MVI L,STAT
725      60A7      7E                                     MOV A,M
726      60A8      4F                                     MOV C,A
727      60A9      E6 10                                     ANI EOIBIT      ;EOI TRUE?
728      60AB      CA 58 61                                JZ  ERR106      ;NO,ERROR
729      60AE      79                                     MOV A,C
730      60AF      E6 40                                     ANI DMAACT      ;DMA STILL ACTIVE?
731      60B1      C2 5D 61                                JNZ  ERR107      ;YES, ERROR
732      60B4      2E 41                                     MVI L,BUFADR    ;RAM ADDR CORRECT?
733      60B6      7E                                     MOV A,M
734      60B7      FE 10                                     CPI 20Q
735      60B9      C2 62 61                                JNZ  ERR108      ;NO
736      60BC      2E 00                                     MVI L,LPHIRO    ;PHI STILL NEEDS DATA?
737      60BE      7E                                     MOV A,M
738      60BF      E6 08                                     ANI OTFIFO
739      60C1      C2 67 61                                JNZ  ERR109      ;YES, ERROR
740      60C4      C3 53 60                                JMP  WRI020

```

=====				SAMPLE HP-IB DRIVER - 13255-91128		PAGE 20
ITEM	LOC	OBJECT CODE	SOURCE STATEMENTS	=====		
742			;			
743			; RDDMA - READ DMA INTERRUPT ROUTINE			
744			;			
745	60C7		RDDMA EQU \$			
746	60C7	C5	PUSH B			
747	60C8	26 88	MVI H,HPIB ;CHECK COMPLETION STATUS			
748	60CA	2E 40	MVI L,STAT			
749	60CC	7E	MOV A,M			
750	60CD	4F	MOV C,A			
751	60CE	E6 10	ANI EOIBIT ;EOI TRUE?			
752	60D0	CA 67 61	JZ ERR109 ;NO,ERROR			
753	60D3	79	MOV A,C			
754	60D4	E6 40	ANI DMAACT ;DMA STILL ACTIVE?			
755	60D6	C2 6C 61	JNZ ERR110 ;YES, ERROR			
756	60D9	2E 41	MVI L,BUFADR ;BUFFER ADDR CORRECT?			
757	60DB	7E	MOV A,M			
758	60DC	FE 20	CPI 400			
759	60DE	C2 71 61	JNZ ERR111 ;NO			
760	60E1	2E 40	MVI L,STAT ;RESET RAM ADDR			
761	60E3	36 10	MVI M,RSTBUF			
762	60E5	0E 0F	MVI C,TSTCHR			
763	60E7		RDMA10 EQU \$			
764	60E7	2E 20	MVI L,BUFRD ;READ A BYTE			
765	60E9	7E	MOV A,M			
766	60EA	B9	CMP C ;COMPARES WITH WHAT IT			
767	60EB	C2 76 61	JNZ ERR112 ;NO			
768	60EE	0D	DCR C ;FINISHED?			
769	60EF	F2 E7 60	JP RDMA10 ;NO			
770	60F2	0E 0F	MVI C,TSTCHR			
771	60F4		RDMA20 EQU \$			
772	60F4	2E 20	MVI L,BUFRD ;READ BYTES XFERRED			
773	60F6	7E	MOV A,M			
774	60F7	47	MOV B,A ; BY DMA TO RAM			
775	60F8	2E 40	MVI L,STAT ;DATA BYTE?			
776	60FA	7E	MOV A,M			
777	60FB	E6 03	ANI D0+D1			
778	60FD	C2 0C 61	JNZ RDMA30 ;NO			
779	6100	78	MOV A,B ;YES			
780	6101	B9	CMP C ;CORRECT DATA?			
781	6102	C2 7B 61	JNZ ERR113 ;NO			
782	6105	0D	DCR C ;YES, GOTO NEXT BYTE			
783	6106	F2 F4 60	JP RDMA20 ;PAST LAST BYTE?			
784	6109	C3 80 61	JMP ERR114 ;YES			
785			;			
786	610C		RDMA30 EQU \$			
787	610C	FE 03	CPI EOITYP ;EOI BYTE?			
788	610E	78	MOV A,B			
789	610F	C2 85 61	JNZ ERR115 ;NO			
790	6112	B7	ORA A ;YES, LAST BYTE?			
791	6113	C2 8A 61	JNZ ERR116 ;NO, ERROR			
792	6116	2E 00	MVI L,LPHIRO ;YES, FIFO STILL NOT			
793	6118	7E	MOV A,M			
794	6119	E6 04	ANI INFIFO ; EMPTY?			
795	611B	C2 8F 61	JNZ ERR117 ;YES, ERROR			
796	611E	C3 53 60	JMP WRI020			

```

=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                SAMPLE HP-IB DRIVER - 13255-91128      PAGE  21
=====
798                                     ;
799                                     ; IDLE - HANDLE ANY EXTRANEIOUS INTERRRUPTS
800                                     ;
801      6121                                     IDLE  EQU  $
802      6121      C5                                     PUSH B
803      6122      2E 00                                     MVI  L,LPHIRO ;SAVE THE STATUS BITS
804      6124      7E                                     MOV  A,M
805      6125      32 5C FE                                STA  FLGSAV
806      6128      2E 40                                     MVI  L,STAT
807      612A      7E                                     MOV  A,M
808      612B      32 5B FE                                STA  FLGSV1
809      612E      3E 04                                     MVI  A,IDLERR ;SET IDLE INTERRUPT
810      6130      21 56 FE                                LXI  H,HIBSTT
811      6133      B6                                     ORA  M
812      6134      77                                     MOV  M,A
813      6135      C1                                     POP  B
814      6136      E1                                     POP  H
815      6137      F1                                     POP  PSW
816      6138      FB                                     EI
817      6139      C9                                     RET
=====

```

=====				SAMPLE HP-IB DRIVER - 13255-91128		PAGE 22
ITEM	LOC	OBJECT CODE	SOURCE STATEMENTS	=====		
819	613A		ERRI00 EQU \$			
820	613A	06 30	MVI B,ZERO			
821	613C	C3 91 61	JMP ERRORI			
822			;			
823	613F		ERRI01 EQU \$			
824	613F	06 31	MVI B,ONE			
825	6141	C3 91 61	JMP ERRORI			
826			;			
827	6144		ERRI02 EQU \$			
828	6144	06 32	MVI B,TWO			
829	6146	C3 91 61	JMP ERRORI			
830			;			
831	6149		ERRI03 EQU \$			
832	6149	06 33	MVI B,THREE			
833	614B	C3 91 61	JMP ERRORI			
834			;			
835	614E		ERRI04 EQU \$			
836	614E	06 34	MVI B,FOUR			
837	6150	C3 91 61	JMP ERRORI			
838			;			
839	6153		ERRI05 EQU \$			
840	6153	06 35	MVI B,FIVE			
841	6155	C3 91 61	JMP ERRORI			
842			;			
843	6158		ERRI06 EQU \$			
844	6158	06 36	MVI B,SIX			
845	615A	C3 91 61	JMP ERRORI			
846			;			
847	615D		ERRI07 EQU \$			
848	615D	06 37	MVI B,SEVEN			
849	615F	C3 91 61	JMP ERRORI			
850			;			
851	6162		ERRI08 EQU \$			
852	6162	06 38	MVI B,EIGHT			
853	6164	C3 91 61	JMP ERRORI			
854			;			
855	6167		ERRI09 EQU \$			
856	6167	06 39	MVI B,NINE			
857	6169	C3 91 61	JMP ERRORI			
858			;			
859	616C		ERRI10 EQU \$			
860	616C	06 3A	MVI B,TEN			
861	616E	C3 91 61	JMP ERRORI			
862			;			
863	6171		ERRI11 EQU \$			
864	6171	06 3B	MVI B,ELEVEN			
865	6173	C3 91 61	JMP ERRORI			
866			;			
867	6176		ERRI12 EQU \$			
868	6176	06 3C	MVI B,TWELVE			
869	6178	C3 91 61	JMP ERRORI			
870			;			
871	617B		ERRI13 EQU \$			
872	617B	06 3D	MVI B,THRTEEN			
873	617D	C3 91 61	JMP ERRORI			
874			;			
	6180		ERRI14 EQU \$			

```

=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                                SAMPLE HP-IB DRIVER - 13255-91128      PAGE 23
=====
876      6180      06 3E          MVI B,FORTEN
877      6182      C3 91 61      JMP ERRORI
878
879      6185          ;
ERRI15 EQU $
880      6185      06 3F          MVI B,FIVTEN
881      6187      C3 91 61      JMP ERRORI
882
883      618A          ;
ERRI16 EQU $
884      618A      06 40          MVI B,SIXTEN
885      618C      C3 91 61      JMP ERRORI
886
887      618F          ;
ERRI17 EQU $
888      618F      06 41          MVI B,SEVTEN
889
890          ;
; ERRORI - HANDLE ERROR MESSAGES
891          ;
892      6191          ERRORI EQU $
893      6191      78              MOV A,B
894      6192      32 57 FE      STA HIBERR
895      6195      21 21 61      LXI H,IDLE
896      6198      22 59 FE      SHLD HIBVEC
897      619B      3A 56 FE      LDA HIBSTT
898      619E      E6 FC          ANI ONES-ERRINT-FIN
899      61A0      F6 03          ORI ERRINT+FIN
900      61A2      32 56 FE      STA HIBSTT
901      61A5      C1              POP B
902      61A6      E1              POP H
903      61A7      F1              POP PSW
904      61A8      FB              EI
905      61A9      C9              RET
; RETURN CLEANLY

```



```

=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                                SAMPLE HP-IB DRIVER - 13255-91128      PAGE  24
=====
907      ;
908      ;
909      ; STATUS ROUTINE
910      ;
911      ;
912      61AA      STAPTP EQU $
913      61AA      21 EA 62      LXI H,UP
914      61AD      E5            PUSH H
915      61AE      21 B8 61      LXI H,STATBL
916      61B1      3A 60 FE      LDA STYPE
917      61B4      3D            DCR A ;ADJUST FOR TABLE INDEX
918      61B5      C3 12 63      JMP SETJMP
919      ;
920      61B8      STATBL EQU $
921      61B8      BE 61          DW STAT1
922      61BA      F7 61          DW STAT2
923      61BC      3C 62          DW STAT3
924      ;
925      ; STAT1 - RETURN GENERAL HP-IB INFO
926      ;
927      61BE      STAT1 EQU $
928      61BE      3A 5D FE      LDA STRT2 ;RETURN TIME-OUT STATUS
929      61C1      FE 41          CPI TIMERR
930      61C3      3E 00          MVI A,0
931      61C5      C2 CA 61      JNZ STAT10
932      61C8      3E 04          MVI A,40
933      61CA      STAT10 EQU $
934      61CA      32 49 FF      STA IOSTA1
935      61CD      AF            XRA A
936      61CE      32 5D FE      STA STRT2
937      61D1      06 00          MVI B,0
938      61D3      3A 62 FE      LDA SRQADR
939      61D6      B7            ORA A ;ANSWERED SRQ STATUS
940      61D7      F2 DC 61      JP STAT12 ;NO
941      61DA      06 01          MVI B,1
942      61DC      STAT12 EQU $
943      61DC      3A 61 FE      LDA PPADR ;CHECK PARALLEL POLL STATUS
944      61DF      B7            ORA A
945      61E0      3E 00          MVI A,0
946      61E2      CA E7 61      JZ STAT14 ;NO PARALLEL POLL PENDING
947      61E5      3E 02          MVI A,20
948      61E7      STAT14 EQU $
949      61E7      B0            ORA B
950      61E8      32 4A FF      STA IOSTA2
951      61EB      3A 03 88      LDA PHIRG3 ;RETURN CURRENT PHI MODES
952      61EE      E6 38          ANI REMOTE+CIC+SYSCTL
953      61F0      0F            RRC
954      61F1      0F            RRC
955      61F2      0F            RRC
956      61F3      32 4B FF      STA IOSTA3
957      61F6      C9            RET

```

```

=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                SAMPLE HP-IB DRIVER - 13255-91128      PAGE 25
=====
959                      ;
960                      ; STAT2 - RETURN STATUS ASSOCIATED WITH SRQ
961                      ;
962      61F7      STAT2 EQU $
963      61F7      3A 62 FE      LDA SRQADR      ;ANSWERED ANY SRQ?
964      61FA      B7              ORA A
965      61FB      FA 06 62      JM STAT22      ;YES
966      61FE      AF              XRA A
967      61FF      4F              MOV C,A
968      6200      32 49 FF      STA IOSTA1      ;NO, CLEAR THE STATUS
969      6203      C3 1E 62      JMP STAT24
970                      ;
971      6206      STAT22 EQU $
972      6206      3A 5F FE      LDA SRQSTA      ;GET STATUS BYTE FROM SRQ DEVICE
973      6209      47              MOV B,A
974      620A      E6 F8          ANI 370Q      ;EXTRACT THESE STATUS BITS AND SAVE
975      620C      0F              RRC
976      620D      0F              RRC
977      620E      0F              RRC
978      620F      4F              MOV C,A
979      6210      E6 10          ANI 20Q
980      6212      0F              RRC
981      6213      B1              ORA C
982      6214      E6 0F          ANI 17Q
983      6216      32 49 FF      STA IOSTA1
984      6219      78              MOV A,B
985      621A      E6 07          ANI 7Q
986      621C      07              RLC
987      621D      4F              MOV C,A
988      621E      STAT24 EQU $
989      621E      3A 62 FE      LDA SRQADR      ;GET SRQ ADDRESS AND PUT IN STATUS AREA
990      6221      47              MOV B,A
991      6222      E6 10          ANI 20Q
992      6224      0F              RRC
993      6225      0F              RRC
994      6226      0F              RRC
995      6227      0F              RRC
996      6228      B1              ORA C
997      6229      32 4A FF      STA IOSTA2
998      622C      AF              XRA A
999      622D      32 5F FE      STA SRQSTA
1000     6230      78              MOV A,B
1001     6231      E6 0F          ANI 17Q
1002     6233      32 4B FF      STA IOSTA3
1003     6236      3E 1F          MVI A,31
1004     6238      32 62 FE      STA SRQADR
1005     623B      C9              RET
=====

```

```

=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                SAMPLE HP-IB DRIVER - 13255-91128      PAGE 26
=====
1007                      ;
1008                      ; STAT3 - RETURN STATUS ASSOCIATED WITH PARALLEL POLL
1009                      ;
1010      623C                      STAT3 EQU S
1011      623C      3A 61 FE      LDA PPADR
1012      623F      47                      MOV B,A
1013      6240      E6 F0                      ANI 3600
1014      6242      32 49 FF      STA IOSTA1
1015      6245      78                      MOV A,B
1016      6246      E6 0F                      ANI 170
1017      6248      32 4A FF      STA IOSTA2
1018      624B      3A 03 88      LDA PHIRG3
1019      624E      E6 06                      ANI P3LSTN+P3TALK
1020      6250      0F                      HRC
1021      6251      32 4B FF      STA IOSTA3
1022      6254      AF                      XRA A
1023      6255      32 61 FE      STA PPADR
1024      6258      C9                      RET
=====

```

=====				SAMPLE HP-IB DRIVER - 13255-91128		PAGE 27
ITEM	LOC	OBJECT CODE	SOURCE STATEMENTS	=====		
1026			;			
1027			; * * * * *			
1028			;			
1029			; PTPINI, PTPIN2 - INITIALIZE HP-IB			
1030			;			
1031			; ENTRY: CALLED ON HARD RESET			
1032			;			
1033			; EXIT :			
1034			;			
1035			; NC => NO ERROR			
1036			; A, B, C, H, L DESTROYED			
1037			;			
1038			;			
1039	6259		PTPINI EQU \$			
1040	6259	3E C3	MVI A, JMP			
1041	625B	32 68 91	STA SCNVEC ;PUT POINTER TO ROUTINE FOR			
1042	625E	21 6E 6B	LXI H, CHARIN ; NON-CONTROLLER APP'S			
1043	6261	22 69 91	SHLD SCNVEC+1			
1044	6264		PTPI02 EQU \$			
1045	6264	26 88	MVI H, HPIB ;POWER-ON PCA TO KNOWN STATE			
1046	6266	2E 40	MVI L, CNTL			
1047	6268	36 41	MVI M, PON+RSTDMA			
1048	626A	2E 04	MVI L, LPHIR4 ;TURN ON IFC AND REN			
1049	626C	36 30	MVI M, IFC+REN			
1050	626E		PTPI05 EQU \$			
1051	626E	2E 42	MVI L, READJP			
1052	6270	7E	MOV A, M			
1053	6271	32 7A 91	STA ADDRST			
1054	6274	E6 1F	ANI ADRMSK			
1055	6276	F6 80	ORI ONLINE ;GO ON-LINE			
1056	6278	2E 05	MVI L, LPHIR5			
1057	627A	77	MOV M, A			
1058	627B	0E 14	MVI C, GETCTL ;WAIT 100 MICROSEC			
1059	627D		PTPI10 EQU \$			
1060	627D	0D	DCR C			
1061	627E	C2 7D 62	JNZ PTPI10			
1062	6281	2E 00	MVI L, LPHIR0 ;CLEAR STATUS CHANGE ON GOING TO 'REMOTE'			
1063	6283	36 80	MVI M, STCHNG			
1064	6285	2E 04	MVI L, LPHIR4 ;CLEAR IFC			
1065	6287	36 20	MVI M, REN			
1066	6289	2E 03	MVI L, LPHIR3 ;CONTROLLER IN CHARGE?			
1067	628B	7E	MOV A, M			
1068	628C	E6 10	ANI CIC			
1069	628E	CA 9C 62	JZ PTPI20			
1070	6291	2E 06	MVI L, LPHIR6 ;YES, ENABLE PARALLEL POLL			
1071	6293	36 FF	MVI M, ONES ; MASKS			
1072	6295	2E 00	MVI L, LPHIR0			
1073	6297	36 80	MVI M, STCHNG			
1074	6299	C3 A4 62	JMP PTPI30			
1075	629C		PTPI20 EQU \$			
1076	629C	3A 7A 91	LDA ADDRST			
1077	629F	E6 20	ANI LA ;NON-CONTROLLER MODE ACCESS?			
1078	62A1	C4 64 63	CNZ NCON ;YES			
1079	62A4		PTPI30 EQU \$			
1080	62A4	2E 40	MVI L, CNTL ;ENABLE HP-IB ATN TO PHI			
1081	62A6	36 02	MVI M, ATNENB			
1082	62A8	32 73 91	STA CNTLWD			

```

=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                                SAMPLE HP-IB DRIVER = 13255-9112#      PAGE  28
=====
1083      62AB      3E 00                      MVI  A,0
1084      62AD      32 6D 91                    STA  FLAGS2
1085      62B0      3E 01                      MVI  A,1
1086      62B2      32 60 FE                    STA  STYPE
1087      62B5      3E 1E                      MVI  A,TERMD ;DEFAULT ADDR OF TALKER AND LISTENER
1088      62B7      32 76 91                    STA  ADRTLK  ; TO TERMINAL
1089      62BA      32 78 91                    STA  ADRLIS
1090      62BD      3E 1F                      MVI  A,31
1091      62BF      32 62 FE                    STA  SRQADR  ;PRESET SRQ RESPONSE=NO
1092      62C2      3E 80                      MVI  A,NOSEC ;INDICATE NO SECONDARY AVAILABLE
1093      62C4      32 77 91                    STA  LISSEC
1094      62C7      32 75 91                    STA  TLKSEC
1095      62CA      2E 01                      MVI  L,LPHIR1 ;ENABLE ALL FLAGS
1096      62CC      36 FF                      MVI  M,ONES
1097      62CE      21 21 61                    LXI  H,IDLE  ;SET INTERRUPT VECTOR
1098      62D1      22 59 FE                    SHLD HIBVEC
1099      62D4      01 00 00                    LXI  B,0     ;NO BUFFER REQUIRED
1100      62D7      C9                          RET
1101                                     ;
1102                                     ;  INITIALIZATION CONTINUATOR
1103                                     ;
1104      62D8                                     PTPIN2 EQU  $
1105      62D8      B7                                     ORA  A           ;NC => NO ERROR
1106      62D9      C9                          RET

```

```

=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                                SAMPLE HP-IB DRIVER - 13255-91128      PAGE  29
=====
1108      ;
1109      ; * * * * *
1110      ;
1111      ;      PTPCTR - CONTROL HP-IB DEVICE
1112      ;
1113      ;      ENTRY:  IOCTYP = TYPE OF CONTROL CALL
1114      ;                  IOCCNT = 2-BYTE DATA WORD
1115      ;
1116      ;      EXIT :  A,B,C DESTROYED
1117      ;                  NC, IOCERR=S => SUCCESS
1118      ;                  C, IOCERR=F => DISPLAY MESSAGE
1119      ;                      (NOT NECESSARILY FAILURE)
1120      ;                  IOCTYP = 0 (REWIND) =>
1121      ;                      DO POWER ON INIT
1122      ;
1123      ;                  IOCTYP = 1 (SKIP LINE) =>
1124      ;                      SET TALKER ADDR OF HP-IB DEV
1125      ;
1126      ;                  IOCTYP = 2 (FIND FILE) =>
1127      ;                      SET LISTENER ADDR OF HP-IB DEV
1128      ;
1129      ;                  IOCTYP = 5 (MARK FILE) =>
1130      ;                      DO SELF TEST
1131      ;
1132      62DA      PTPCTR EQU $
1133      62DA      21 EA 62      LXI H,UP
1134      62DD      E5      PUSH H
1135      62DE      21 F1 62      LXI H,CTLTBL
1136      62E1      3A D8 FF      LDA IOCTYP
1137      62E4      FE 0B      CPI 11
1138      62E6      DA 12 63      JC SETJMP
1139      62E9      UP0 EQU $
1140      62E9      E1      POP H
1141      62EA      UP EQU $
1142      62EA      3E 53      MVI A,S
1143      62EC      32 4F FF      STA IOCERR
1144      62EF      B7      ORA A
1145      62F0      C9      RET
1146      ;
1147      ;      CTLTBL - FUNCTIONS AVAILABLE
1148      ;
1149      62F1      CTLTBL EQU $
1150      62F1      64 62      DW PTP102
1151      62F3      3D 6B      DW TLKR00
1152      62F5      0C 6B      DW LSTN00
1153      62F7      07 63      DW XFUNG
1154      62F9      EA 62      DW UP
1155      62FB      40 64      DW TEST
1156      62FD      D6 63      DW PP0000
1157      62FF      F4 63      DW SRQ000
1158      6301      25 64      DW XEOIOT
1159      6303      2E 64      DW XDATOT
1160      6305      37 64      DW COMOUT

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=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                                SAMPLE HP-IB DRIVER - 13255-91128      PAGE 30
=====
1162      ;
1163      ; XFUNC - DETERMINE TYPE OF CONTROL FUNCTION
1164      ; REQUESTED AND EXECUTE IT
1165      ;
1166      6307      XFUNC EQU $
1167      6307      21 1C 63      LXI H,XFNTBL
1168      630A      3A D5 FF      LDA IOCCNT
1169      630D      FE 10      CPI 16
1170      630F      D2 E9 62      JNC UP0
1171      6312      SETJMP EQU $
1172      6312      87      ADD A
1173      6313      4F      MOV C,A
1174      6314      06 00      MVI B,0
1175      6316      09      DAD B
1176      6317      7E      MOV A,M
1177      6318      23      INX H
1178      6319      66      MOV H,M
1179      631A      6F      MOV L,A
1180      631B      E9      PCHL
1181      ;
1182      ; XFNTBL - EXTRA FUNCTIONS
1183      ;
1184      631C      XFNTBL EQU $
1185      631C      3C 63      DW MDNON
1186      631E      50 63      DW MDNDFF
1187      6320      64 63      DW NCON
1188      6322      6D 63      DW NCOFF
1189      6324      76 63      DW REENDN
1190      6326      7F 63      DW REENDFF
1191      6328      88 63      DW IFCON
1192      632A      91 63      DW IFCDFF
1193      632C      9A 63      DW SRQON
1194      632E      A3 63      DW SRQOFF
1195      6330      AC 63      DW PPDN
1196      6332      B5 63      DW PPOFF
1197      6334      BE 63      DW XSTAT1
1198      6336      C4 63      DW XSTAT2
1199      6338      CA 63      DW XSTAT3
1200      633A      D0 63      DW XSTAT4
=====

```

```

=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                                SAMPLE HP-IB DRIVER - 13255-91128      PAGE 31
=====
1202      ;
1203      ; MONON - ENABLE MONITOR MODE, THIS ALLOWS THE
1204      ;   TERMINAL TO SEE ALL HP-IB COMMANDS AND DATA
1205      ;   THAT ARE BEING PLACED ON THE HP-IB.
1206      ;
1207      633C      MONON EQU $
1208      633C      26 88      MVI H,HPIB
1209      633E      3A 73 91    LDA CNTLWD      ;DISABLE THE HP-IB ATN LINE TO THE PHI
1210      6341      E6 FD      ANI ONES-ATNENB
1211      6343      2E 40      MVI L,CNTL
1212      6345      77      MOV M,A
1213      6346      32 73 91    STA CNTLWD
1214      6349      2E 05      MVI L,LPHIR5      ;SET UP PHI TO LISTEN ALWAYS
1215      634B      7E      MOV A,M
1216      634C      F6 20      ORI LA
1217      634E      77      MOV M,A
1218      634F      C9      RET      ;EXIT SUCCESSFULLY
1219      ;
1220      ; MONOFF - DISABLE MONITOR MODE, RETURN TO NORMAL
1221      ;   HP-IB OPERATION AND DISPLAY DATA ONLY WHEN
1222      ;   ADDRESSED.
1223      ;
1224      6350      MONOFF EQU $
1225      6350      26 88      MVI H,HPIB
1226      6352      3A 73 91    LDA CNTLWD      ;RE-ENABLE THE HP-IB ATN LINE TO THE PHI
1227      6355      F6 02      ORI ATNENB
1228      6357      32 73 91    STA CNTLWD
1229      635A      2E 40      MVI L,CNTL
1230      635C      77      MOV M,A      ;RETURN PHI TO NORMAL LISTEN OPERATION
1231      635D      2E 05      MVI L,LPHIR5
1232      635F      7E      MOV A,M
1233      6360      E6 DF      ANI ONES-LA
1234      6362      77      MOV M,A
1235      6363      C9      RET
1236      ;
1237      ; NCON - ENABLE NON-CONTROLLER MODE
1238      ;
1239      6364      NCON EQU $
1240      6364      3A 74 91    LDA IBFLGS
1241      6367      F6 02      ORI NCM
1242      6369      32 74 91    STA IBFLGS
1243      636C      C9      RET
1244      ;
1245      ; NCOFF - DISABLE NON-CONTROLLER MODE
1246      ;
1247      636D      NCOFF EQU $
1248      636D      3A 74 91    LDA IBFLGS
1249      6370      E6 FD      ANI ONES-NCM
1250      6372      32 74 91    STA IBFLGS
1251      6375      C9      RET

```



```

=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                                SAMPLE HP-IB DRIVER - 13255-91128      PAGE 32
=====
1253      ;
1254      ; RENON - ENABLE HP-IB REN LINE
1255      ;
1256      6376      RENON EQU $
1257      6376      26 88      MVI H,HPIB
1258      6378      2E 04      MVI L,LPHIR4
1259      637A      7E      MOV A,M
1260      637B      F6 20      ORI REN
1261      637D      77      MOV M,A
1262      637E      C9      RET
1263      ;
1264      ; RENOFF - DISABLE HP-IB REN LINE
1265      ;
1266      637F      RENOFF EQU $
1267      637F      26 88      MVI H,HPIB
1268      6381      2E 04      MVI L,LPHIR4
1269      6383      7E      MOV A,M
1270      6384      E6 DF      ANI ONES-REN
1271      6386      77      MOV M,A
1272      6387      C9      RET
1273      ;
1274      ; IFCON - ENABLE HP-IB IFC LINE
1275      ;
1276      6388      IFCON EQU $
1277      6388      26 88      MVI H,HPIB
1278      638A      2E 04      MVI L,LPHIR4
1279      638C      7E      MOV A,M
1280      638D      F6 10      ORI IFC
1281      638F      77      MOV M,A
1282      6390      C9      RET
1283      ;
1284      ; IFCOFF - DISABLE HP-IB IFC LINE
1285      ;
1286      6391      IFCOFF EQU $
1287      6391      26 88      MVI H,HPIB
1288      6393      2E 04      MVI L,LPHIR4
1289      6395      7E      MOV A,M
1290      6396      E6 EF      ANI ONES-IFC
1291      6398      77      MOV M,A
1292      6399      C9      RET
=====

```

```

=====
ITEM    LOC    OBJECT CODE    SOURCE STATEMENTS                                SAMPLE HP-IB DRIVER - 13255-91128    PAGE 33
=====
1294                                          ;
1295                                          ; SRQON - SIGNAL SERVICE VIA SRQ ON HP-IB
1296                                          ;
1297    639A                                          SRQON EQU $
1298    639A    26 88                                MVI H,HPIB
1299    639C    2E 04                                MVI L,LPHIR4
1300    639E    7E                                MOV A,M
1301    639F    F6 04                                ORI SRQOUT
1302    63A1    77                                MOV M,A
1303    63A2    C9                                RET
1304                                          ;
1305                                          ; SRQOFF - REMOVE SERVICE REQUEST FROM HP-IB
1306                                          ;
1307    63A3                                          SRQOFF EQU $
1308    63A3    26 88                                MVI H,HPIB
1309    63A5    2E 04                                MVI L,LPHIR4
1310    63A7    7E                                MOV A,M
1311    63A8    E6 FB                                ANI ONES-SRQOUT
1312    63AA    77                                MOV M,A
1313    63AB    C9                                RET
1314                                          ;
1315                                          ; PPON - REQUEST SERVICE VIA PARALLEL POLL ON HP-IB
1316                                          ;
1317    63AC                                          PPON EQU $
1318    63AC    26 88                                MVI H,HPIB
1319    63AE    2E 04                                MVI L,LPHIR4
1320    63B0    7E                                MOV A,M
1321    63B1    F6 08                                ORI PPOUT
1322    63B3    77                                MOV M,A
1323    63B4    C9                                RET
1324                                          ;
1325                                          ; PPOFF - REMOVE PARALLEL POLL REQUEST FROM HP-IB
1326                                          ;
1327    63B5                                          PPOFF EQU $
1328    63B5    26 88                                MVI H,HPIB
1329    63B7    2E 04                                MVI L,LPHIR4
1330    63B9    7E                                MOV A,M
1331    63BA    E6 F7                                ANI ONES-PPOUT
1332    63BC    77                                MOV M,A
1333    63BD    C9                                RET
=====

```

```

=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                                SAMPLE HP-IB DRIVER = 13255-91128      PAGE  34
=====
1335                                           ;
1336                                           ;  XSTAT1,XSTAT2,XSTAT3,XSTAT4 - SET UP TYPE OF STATUS RETURN
1337                                           ;
1338      63BE                                           XSTAT1 EQU  $
1339      63BE      3E 01                               MVI  A,1
1340      63C0      32 60 FE                             STA  STYPE
1341      63C3      C9                                   RET
1342                                           ;
1343      63C4                                           XSTAT2 EQU  $
1344      63C4      3E 02                               MVI  A,2
1345      63C6      32 60 FE                             STA  STYPE
1346      63C9      C9                                   RET
1347                                           ;
1348      63CA                                           XSTAT3 EQU  $
1349      63CA      3E 03                               MVI  A,3
1350      63CC      32 60 FE                             STA  STYPE
1351      63CF      C9                                   RET
1352                                           ;
1353      63D0                                           XSTAT4 EQU  $
1354      63D0      3E 04                               MVI  A,4
1355      63D2      32 60 FE                             STA  STYPE
1356      63D5      C9                                   RET

```

```

=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                                SAMPLE HP-IB DRIVER - 13255-91120      PAGE 35
=====
1358                                           ;
1359                                           ; PP0000 - SET PARALLEL MASK BIT CORRESPONDING
1360                                           ; TO HP-IB ADDRESS
1361                                           ;
1362      63D6      PP0000 EQU $
1363      63D6      3A D5 FF      LDA IOCCNT      ;GREATER THAN 8?
1364      63D9      FE 08      CPI 8
1365      63DB      D2 EF 63      JNC PP030      ;YES, CLEAR
1366      63DE      21 63 FE      LXI H,PPBYTE
1367      63E1      4F      MOV C,A
1368      63E2      3E 80      MVI A,2000
1369      63E4      PP010 EQU $
1370      63E4      0D      DCR C
1371      63E5      FA EC 63      JM PP020
1372      63E8      0F      RRC
1373      63E9      C3 E4 63      JMP PP010
1374                                           ;
1375      63EC      PP020 EQU $
1376      63EC      B6      ORA M      ;MERGE WITH CURRENT VALUES
1377      63ED      77      MOV M,A
1378      63EE      C9      RET
1379                                           ;
1380      63EF      PP030 EQU $
1381      63EF      AF      XRA A
1382      63F0      32 63 FE      STA PPBYTE
1383      63F3      C9      RET
=====

```

```

=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                SAMPLE HP-IB DRIVER = 13255-91128      PAGE 36
=====
1385      ;
1386      ;
1387      ; SRQ000 - ADD NEW HP-IB ADDRESS TO SRQ SEARCH TABLE
1388      ;
1389      63F4      SRQ000 EQU $
1390      63F4      3A D5 FF      LDA IOCCNT      ;GREATER THAN 31?
1391      63F7      FE 1F          CPI 31
1392      63F9      D2 18 64      JNC SRQ100      ;YES, CLEAR SRQ TABLE
1393      63FC      21 64 FE      LXI H,SRQTBL
1394      63FF      SRQ010 EQU $
1395      63FF      FE 08          CPI 8          ;CONVERT NUMBER TO BIT POSITION WITHIN TABLE
1396      6401      DA 0A 64      JC SRQ020
1397      6404      23            INX H
1398      6405      D6 08          SUI 8
1399      6407      C3 FF 63      JMP SRQ010
1400      ;
1401      640A      SRQ020 EQU $
1402      640A      4F            MOV C,A
1403      640B      3E 01          MVI A,1
1404      640D      SRQ030 EQU $
1405      640D      0D            DCR C
1406      640E      FA 15 64      JM SRQ040
1407      6411      07            RLC
1408      6412      C3 0D 64      JMP SRQ030
1409      ;
1410      6415      SRQ040 EQU $
1411      6415      B6            ORA M
1412      6416      77            MOV M,A
1413      6417      C9            RET
1414      ;
1415      6418      SRQ100 EQU $
1416      6418      21 64 FE      LXI H,SRQTBL ;CLEAR 4 BYTES OF SRQ BIT TABLE
1417      641B      AF            XRA A
1418      641C      0E 04          MVI C,4
1419      641E      SRQ110 EQU $
1420      641E      77            MOV M,A
1421      641F      23            INX H
1422      6420      0D            DCR C
1423      6421      C2 1E 64      JNZ SRQ110
1424      6424      C9            RET
=====

```

```

=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                SAMPLE HP-IB DRIVER - 13255-91128      PAGE 37
=====
1426                      ;
1427                      ; XEOIOT - OUTPUT DATA BYTE WITH EOI TRUE, ASSUMES TERMINAL
1428                      ; IS CURRENTLY ADDRESSED TO TALK
1429                      ;
1430      6425          XEOIOT EQU $
1431      6425      3A D5 FF          LDA IOCCNT
1432      6428      CD 8A 6E          CALL EOIOU
1433      642B      D0                  RNC
1434      642C      E1                  POP H
1435      642D      C9                  RET
1436                      ;
1437                      ; XDATOT - OUTPUT DATA BYTE, ASSUMES TERMINAL IS TALKER
1438                      ;
1439      642E          XDATOT EQU $
1440      642E      3A D5 FF          LDA IOCCNT
1441      6431      CD 66 6E          CALL DATAOT
1442      6434      D0                  RNC
1443      6435      E1                  POP H
1444      6436      C9                  RET
1445                      ;
1446                      ; COMOUT - OUTPUT HP-IB COMMAND
1447                      ;
1448      6437          COMOUT EQU $
1449      6437      3A D5 FF          LDA IOCCNT
1450      643A      CD 4C 6F          CALL TLK013
1451      643D      D0                  RNC
1452      643E      E1                  POP H
1453      643F      C9                  RET

```



```

=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                                SAMPLE HP-IB DRIVER - 13255-91128      PAGE 39
=====
1512      645D      CD 9F 69      CALL RDREG      ;READ DATA JUST WRITTEN
1513
1514      ; COMPLEMENT DATA PATTERN AND DO AGAIN
1515      ;
1516      6460      11 09 6A      LXI D,TSTB05
1517      6463      CD 92 69      CALL WRTREG
1518      6466      06 33      MVI B,THREE ;SET TEST FAIL NUMBER
1519      6468      11 14 6A      LXI D,TSTB06
1520      646B      CD 9F 69      CALL RDREG
1521      ;
1522      ; VERIFY REGISTERS ARE ADDRESSABLE
1523      ;
1524      646E      11 1F 6A      LXI D,TSTB07
1525      6471      CD 92 69      CALL WRTREG
1526      6474      06 34      MVI B,FOUR ;SET TEST FAIL NUMBER
1527      6476      11 2A 6A      LXI D,TSTB08
1528      6479      CD 9F 69      CALL RDREG
1529      647C      2E 03      MVI L,LPHIR3 ;IS PHI NOW SYSTEM CTL?
1530      647E      7E      MOV A,M
1531      647F      E6 08      ANI SYCTL
1532      6481      CA C8 69      JZ ERR05 ;NO, ERROR
1533      6484      2E 04      MVI L,LPHIR4 ;ASSERT IFC AND SEE IF
1534      6486      36 10      MVI M,IFC ; PHI BECOMES CONTROLLER
1535      6488      AF      XRA A ; IN CHARGE
1536      6489      77      MOV M,A
1537      648A      2E 03      MVI L,LPHIR3
1538      648C      7E      MOV A,M
1539      648D      E6 10      ANI CIC
1540      648F      CA CD 69      JZ ERR06 ;NO, ERROR
1541      6492      2E 40      MVI L,CNTL ;YES, RE-INIT
1542      6494      36 41      MVI M,PON+RSTDMA
=====

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=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                                SAMPLE HP=1B DRIVER = 13255-91128      PAGE  40
=====
1544      ;
1545      ; TEST 1 - SEE IF PHI WILL TRANSFER
1546      ; ALL 256 POSSIBLE BIT PATTERNS
1547      ;
1548      ; (DONE BY WRITING AND READING ONE
1549      ; BYTE AT A TIME WHILE PHI IS LISTEN-
1550      ; ALWAYS AND TALK ALWAYS...)
1551      ;
1552      6496      TST100 EQU $
1553      6496      3E 31      MVI A,ONE
1554      6498      32 55 FE    STA TESTNO
1555      649B      26 88      MVI H,HPIB ;INITIALIZE FIFO'S
1556      649D      2E 04      MVI L,LPHIR4
1557      649F      36 01      MVI M,INITFF ;SET PHI TO TALK ALWAYS
1558      64A1      2E 05      MVI L,LPHIR5 ; AND LISTEN ALWAYS
1559      64A3      36 60      MVI M,LA+TA ;PHI 'J' BYPASS
1560      64A5      2E 02      MVI L,LPHIR2
1561      64A7      7E         MOV A,M
1562      64A8      2E 03      MVI L,LPHIR3 ;ENABLE DATA FLAGS
1563      64AA      36 01      MVI M,FREEZE
1564      64AC      2E 01      MVI L,LPHIR1
1565      64AE      36 0C      MVI M,INFIFO+OTFIFO
1566      64B0      21 02 88    LXI H,PHIRG2+DATA2
1567      64B3      0E 00      MVI C,0
1568      64B5      TST110 EQU $
1569      64B5      3E 64      MVI A,TIMOUT ;SET TIME OUT COUNTER
1570      64B7      32 79 91    STA XTIMER
1571      64BA      TST120 EQU $
1572      64BA      3A 79 91    LDA XTIMER ;TIME OUT?
1573      64BD      B7         ORA A
1574      64BE      CA AF 69    JZ ERROR ;YES, ERROR
1575      64C1      2E 00      MVI L,LPHIR0 ;PHI NEEDS DATA?
1576      64C3      7E         MOV A,M
1577      64C4      E6 08      ANI OTFIFO
1578      64C6      CA BA 64    JZ TST120 ;NO, CONTINUE WAITING
1579      64C9      TST130 EQU $
1580      64C9      2E 02      MVI L,LPHIR2+DATA2
1581      64CB      71         MOV M,C ;STORE DATA BYTE
1582      64CC      3E 64      MVI A,TIMOUT ;SET TIME OUT
1583      64CE      32 79 91    STA XTIMER
1584      64D1      TST140 EQU $
1585      64D1      3A 79 91    LDA XTIMER ;TIME OUT?
1586      64D4      B7         ORA A
1587      64D5      CA B4 69    JZ ERROR1 ;YES, ERROR
1588      64D8      2E 00      MVI L,LPHIR0 ;DATA AVAILABLE FROM PHI?
1589      64DA      7E         MOV A,M
1590      64DB      E6 04      ANI INFIFO
1591      64DD      CA D1 64    JZ TST140 ;NO, CONTINUE WAITING
1592      64E0      TST150 EQU $
1593      64E0      2E 02      MVI L,LPHIR2
1594      64E2      7E         MOV A,M ;READ THE DATA BYTE
1595      64E3      B9         CMP C ;SAME AS WHAT WAS
1596      64E4      C2 B9 69    JNZ ERROR2 ;NO, ERROR
1597      64E7      0C         INR C ;FINISH ALL 256 BYTES?
1598      64E8      C2 B5 64    JNZ TST110 ;NO

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=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                                SAMPLE HP-IB DRIVER - 13255-91128      PAGE  41
=====
1600      ;
1601      ; TEST 2 - WRITE 16 DATA BYTES DIRECTLY TO
1602      ; PHI CHIP
1603      ;
1604      64EB      TST200 EQU $
1605      64EB      3E 32      MVI A,TWO
1606      64ED      32 55 FE      STA TESTING
1607      64F0      2E 04      MVI L,LPHIR4 ;INITIALIZE THE FIFO'S
1608      64F2      36 01      MVI M,INITFF
1609      64F4      2E 01      MVI L,LPHIR1 ;ENABLE FIFO DATA FLAG
1610      64F6      36 08      MVI M,OTFIFO
1611      64F8      0E 0F      MVI C,TSTCHR ;INITIAL CHARACTER XMIT
1612      64FA      TST210 EQU $
1613      64FA      3E 64      MVI A,TIMOUT ;INITIALIZE TIME-OUT
1614      64FC      32 79 91      STA XTIMER
1615      64FF      TST220 EQU $
1616      64FF      3A 79 91      LDA XTIMER ;TIME OUT?
1617      6502      B7          ORA A
1618      6503      CA AF 69      JZ ERROR00 ;YES, ERROR
1619      6506      2E 00      MVI L,LPHIRO ;PHI NEEDS DATA?
1620      6508      7E          MOV A,M
1621      6509      E6 08      ANI OTFIFO
1622      650B      CA FF 64      JZ TST220 ;NO, CONTINUE WAITING
1623      650E      TST230 EQU $
1624      650E      79          MOV A,C ;GET CHAR TO BE XMIT
1625      650F      B7          ORA A ;LAST CHAR?
1626      6510      CA 1A 65      JZ TST240 ;YES
1627      6513      2E 02      MVI L,LPHIR2+DATA2 ;NO, OUTPUT THIS CHAR
1628      6515      77          MOV M,A
1629      6516      0D          DCR C ;GET NEXT CHARACTER
1630      6517      C3 FA 64      JMP TST210 ;CONTINUE WITH NEXT CHAR
1631      651A      TST240 EQU $
1632      651A      2E 12      MVI L,LPHIR2+EOI2 ;SET EOI STATUS
1633      651C      77          MOV M,A ;DOES OTFIFO STILL INDICATE
1634      651D      2E 00      MVI L,LPHIRO
1635      651F      7E          MOV A,M
1636      6520      E6 08      ANI OTFIFO ; NEED FOR DATA?
1637      6522      C2 B4 69      JNZ ERROR1 ;YES, ERROR SINCE BOTH FIFO'S
1638      ;                      ; ARE FULL
=====

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=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                                     SAMPLE HP-IB DRIVER - 13255-91128      PAGE  42
=====
1640
1641      ; TEST 3 - READ THE 16 BYTES THAT WERE JUST
1642      ; WRITTEN...
1643      ;
1644      6525      TST300 EQU  $
1645      6525      3E 33      MVI  A,THREE      ;DISPLAY TEST MESSAGE
1646      6527      32 55 FE      STA  TESTNO
1647      652A      2E 01      MVI  L,LPHIR1      ;ENABLE INFIFO FLAG
1648      652C      36 04      MVI  M,INFIFO
1649      652E      0E 0F      MVI  C,TSTCHR      ;INIT CHAR FOR COMPARE
1650      6530      TST310 EQU  $
1651      6530      2E 00      MVI  L,LPHIRO      ;DATA AVAILABLE FOR IN-FIFO?
1652      6532      7E          MOV  A,M
1653      6533      E6 04      ANI  INFIFO
1654      6535      CA AF 69      JZ   ERR00      ;NO, ERROR
1655      6538      2E 02      MVI  L,LPHIR2      ;YES, GET BYTE
1656      653A      7E          MOV  A,M
1657      653B      47          MOV  B,A
1658      653C      2E 40      MVI  L,STAT
1659      653E      7F          MOV  A,M
1660      653F      E6 03      ANI  D0+D1      ;CHECK TYPE OF BYTE
1661      6541      FE 00      CPI  IDATA      ;DATA?
1662      6543      C2 52 65      JNZ  TST320      ;NO
1663      6546      78          MOV  A,B      ;YES
1664      6547      B9          CMP  C      ;COMPARE AGAINST EXPECTED
1665      6548      C2 B4 69      JNZ  ERR01      ;NO, ERROR
1666      654B      0D          DCR  C      ;YES, SET NEXT CHAR
1667      654C      F2 30 65      JP   TST310      ;PAST LAST CHAR?
1668      654F      C3 B9 69      JMP  ERR02      ;YES
1669      ;
1670      6552      TST320 EQU  $
1671      6552      FE 03      CPI  IE012      ;EOI BYTE?
1672      6554      78          MOV  A,B
1673      6555      C2 BE 69      JNZ  ERR03      ;NO, ERROR
1674      6558      B7          ORA  A      ;LAST DATA BYTE?
1675      6559      C2 C3 69      JNZ  ERR04      ;NO, ERROR
1676      655C      2E 00      MVI  L,LPHIRO      ;YES, INFIFO STILL NOT EMPTY?
1677      655E      7E          MOV  A,M
1678      655F      E6 04      ANI  INFIFO
1679      6561      C2 C8 69      JNZ  ERR05      ;YES, ERROR

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=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                                SAMPLE HP-IB DRIVER - 13255-91128      PAGE  43
=====
1681      ;
1682      ; TEST 4 - CHECK RAM BUFFER BY WRITING
1683      ; DATA TO IT
1684      ;
1685      6564      TST400 EQU $
1686      6564      3E 34      MVI A,FOUR
1687      6566      32 55 FE      STA TESTNO
1688      6569      2E 40      MVI L,CNTL ;INITIALIZE BUFFER ADDR
1689      6568      36 10      MVI M,RSTBUF ; REG
1690      656D      0E 00      MVI C,0
1691      ;
1692      ; CHECK THE RAM ADDR REG AND STORE THE
1693      ; DATA BYTE CORRESPONDING TO THE
1694      ; RAM BUFFER LOCATION
1695      ;
1696      656F      TST410 EQU $
1697      656F      2E 41      MVI L,BUFADR ;READ THE ADDR REGISTER
1698      6571      7E      MOV A,M
1699      6572      B9      CMP C ;AGREE WITH COUNTER?
1700      6573      C2 AF 69      JNZ ERR00 ;NO, DISPLAY ERROR MSG
1701      6576      79      MOV A,C
1702      6577      2E 20      MVI L,BUFWRT+DATA2 ;STORE DATA BYTE
1703      6579      77      MOV M,A
1704      657A      0C      INR C
1705      657B      79      MOV A,C
1706      657C      FE FF      CPI TSTLST ;LAST BYTE?
1707      657E      C2 6F 65      JNZ TST410 ;NO
1708      6581      TST420 EQU $
1709      6581      2E 41      MVI L,BUFADR ;IS BUFFER ADDR = LAST?
1710      6583      7E      MOV A,M
1711      6584      B9      CMP C
1712      6585      C2 B4 69      JNZ ERR01 ;NO, REPORT ERROR
1713      6588      2E B0      MVI L,BUFWRT+EOI2+ENDBIT ;STORE EOI BYTE
1714      658A      77      MOV M,A

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=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                SAMPLE HP-IB DRIVER - 13255-91128      PAGE  44
=====
1716      ;
1717      ; TEST 5 - READ THE DATA FROM THE RAM BUFFER
1718      ;
1719      658B      TST500 EQU $
1720      658B      3E 35      MVI A,FIVE
1721      658D      32 55 FE    STA TESTNO
1722      6590      2E 40      MVI L,CNTL
1723      6592      36 10      MVI M,RSTBUF
1724      6594      0E 00      MVI C,0
1725      ;
1726      ; READ BACK THE DATA BYTES THAT WERE STORED
1727      ; IN THE RAM BUFFER
1728      ;
1729      6596      TST510 EQU $
1730      6596      2E 20      MVI L,BUFRD ;READ A BYTE
1731      6598      7E          MOV A,M
1732      6599      B9          CMP C ;COMPARES WITH WHAT WAS
1733      659A      C2 AF 69    JNZ ERR00 ;NO, REPORT ERROR
1734      659D      2E 40      MVI L,STAT ;DATA BYTE?
1735      659F      7E          MOV A,M
1736      65A0      E6 03      ANI D0+D1
1737      65A2      CA AD 65    JZ TST520 ;YES, CONTINUE READING
1738      65A5      FE 02      CPI 2Q ;NO, EOI BYTE?
1739      65A7      CA B4 65    JZ TST530 ;CHECK THAT EOI OCCURRED
1740      65AA      C3 B4 69    JMP ERR01 ;REPORT ERROR, INCORRECT
1741      65AD      TST520 EQU $ ; HIGH ORDER BITS
1742      65AD      0C          INR C ;HAS COUNTER ROLLED OVER?
1743      65AE      C2 96 65    JNZ TST510 ;NO, CONTINUE
1744      65B1      C3 B9 69    JMP ERR02
1745      ;
1746      65B4      TST530 EQU $
1747      65B4      3E FF      MVI A,TSTLST ;IS THIS THE LAST CHAR?
1748      65B6      B9          CMP C
1749      65B7      C2 BE 69    JNZ ERR03 ;NO, REPORT ERROR (EOI AT
1750      ; ; WRONG TIME)
1751      65BA      2E 41      MVI L,BUFADR ;HAS COUNTER ROLLED OVER?
1752      65BC      7E          MOV A,M
1753      65BD      FE 00      CPI 0
1754      65BF      CA C3 69    JZ ERR04 ;YES, ERROR

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=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                                SAMPLE HP-IB DRIVER - 13255-91128      PAGE 45
=====
1756      ;
1757      ; TEST 6 - TEST PROCESSOR TO DMA, PHI TO
1758      ; PROCESSOR...
1759      ;
1760      65C2      TST600 EQU $
1761      65C2      3E 36      MVI A, SIX
1762      65C4      32 55 FE      STA TESTNO
1763      65C7      2E 40      MVI L, CNTL
1764      65C9      36 10      MVI M, RSTBUF
1765      65CB      3E 0F      MVI A, TSTCHR
1766      65CD      TST610 EQU $
1767      65CD      2E 20      MVI L, BUFVRT+DATA2 ;PRELOAD RAM BUFFER
1768      65CF      77      MOV M, A
1769      65D0      3D      DCR A
1770      65D1      C2 CD 65      JNZ TST610
1771      65D4      2E B0      MVI L, BUFVRT+EOI2+ENDBIT ;LOAD END CHAR
1772      65D6      77      MOV M, A ;RESET BUFFER ADDR
1773      65D7      2E 40      MVI L, CNTL
1774      65D9      36 10      MVI M, RSTBUF
1775      65DB      2E 04      MVI L, LPHIR4
1776      65DD      36 03      MVI M, INIIFB+DMASEL
1777      65DF      3E 64      MVI A, TIMEOUT
1778      65E1      32 79 91      STA XTIMER
1779      65E4      2E 40      MVI L, CNTL ;ABORT DMA ACTIONS
1780      65E6      36 40      MVI M, RSTDMA
1781      65E8      2E 40      MVI L, STAT ;CHECK FOR DMA INACTIVE
1782      65EA      7E      MOV A, M
1783      65EB      E6 40      ANI DMAACT
1784      65ED      C2 AF 69      JNZ ERROR0 ;DMA ACTIVE, ERROR
1785      65F0      2E 01      MVI L, LPHIR1 ;ENABLE OUT FIFO REQ
1786      65F2      36 08      MVI M, OTFIFO
1787      65F4      2E 40      MVI L, CNTL ;START DMA
1788      65F6      36 04      MVI M, BF2PHI
1789      65F8      TST620 EQU $
1790      65F8      2E 40      MVI L, STAT ;FINISH DATA TRANSFER?
1791      65FA      7E      MOV A, M
1792      65FB      47      MOV B, A
1793      65FC      E6 10      ANI EOIBIT
1794      65FE      C2 11 66      JNZ TST630 ;YES
1795      6601      78      MOV A, B ;NO, DMA STILL ACTIVE?
1796      6602      E6 40      ANI DMAACT
1797      6604      CA B4 69      JZ ERROR1 ;NO, ERROR
1798      6607      3A 79 91      LDA XTIMER ;YES, TIME-OUT?
1799      660A      B7      ORA A
1800      660B      C2 F8 65      JNZ TST620 ;NO, CONTINUE
1801      660E      C3 B9 69      JMP ERROR2 ;YES, REPORT ERROR
1802      ;
1803      6611      TST630 EQU $
1804      6611      2E 00      MVI L, LPHIRO ;DATA STILL NEEDED?
1805      6613      7E      MOV A, M
1806      6614      E6 08      ANI OTFIFO
1807      6616      C2 BE 69      JNZ ERROR3 ;YES, ERROR
1808      6619      2E 40      MVI L, STAT ;DMA STILL ACTIVE?
1809      661B      7E      MOV A, M
1810      661C      E6 40      ANI DMAACT
1811      661E      C2 C3 69      JNZ ERROR4 ;YES, ERROR
1812      6621      2F 01      MVI L, LPHIR1 ;ENABLE IN FIFO FLAGS
=====

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=====
ITEM      LOC      OBJECT CODE      SOURCE STATEMENTS      SAMPLE HP-IB DRIVER - 13255-91128      PAGE 46
=====
1813      6623      36 04                      MVI M,INFIFO
1814      6625      0E 0F                      MVI C,TSTCHR
1815      6627                      TST640 EQU $
1816      6627      2E 00                      MVI L,LPHIRO ;DATA AVAILABLE?
1817      6629      7E                      MOV A,M
1818      662A      E6 04                      ANI INFIFO
1819      662C      06 35                      MVI B,65B
1820      662E      CA 53 69                      JZ ERROR2 ;NO, ERROR
1821      6631      2E 02                      MVI L,LPHIR2 ;YES, GET THE BYTE
1822      6633      7E                      MOV A,M
1823      6634      47                      MOV B,A
1824      6635      2E 40                      MVI L,STAT ;GET TYPE OF BYTE
1825      6637      7E                      MOV A,M
1826      6638      E6 03                      ANI D0+D1
1827      663A      C2 49 66                      JNZ TST650 ;NOT DATA BYTE
1828      663D      78                      MOV A,B ;COMPARES WITH WHAT IT
1829      663E      B9                      CMP C ; SHOULD BE?
1830      663F      C2 CD 69                      JNZ ERR06 ;NO, ERROR
1831      6642      0D                      DCR C ;YES, GO TO NEXT BYTE
1832      6643      F2 27 66                      JP TST640 ;DIDN'T ROLL OVER
1833      6646      C3 D2 69                      JMP ERR07
1834
1835      6649                      ;
1836      6649                      TST650 EQU $
1837      6649      FE 03                      CPI IEOI2 ;EOI BYTE?
1838      664B      78                      MOV A,B
1839      664C      C2 D7 69                      JNZ ERR08 ;NO, ERROR
1840      664F      B7                      ORA A ;YES, LAST BYTE?
1841      6650      C2 DC 69                      JNZ ERR09 ;NO, ERROR
1842      6653      2E 00                      MVI L,LPHIRO ;STILL DATA AVAILABLE?
1843      6655      7E                      MOV A,M
1844      6656      E6 04                      ANI INFIFO
1845      6658      C2 E1 69                      JNZ ERR10 ;YES, ERROR
=====

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=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                                SAMPLE HP-IB DRIVER - 13255-91128      PAGE 47
=====
1846      ;
1847      ; TEST 7 - PROCESSOR TO PHI, PHI TO DMA
1848      ;
1849      665B      TST700 EQU  S
1850      665B      3E 37      MVI  A,SEVEN      ;SET UP TEST 7 MESSAGE
1851      665D      32 55 FE    STA  TESTNO
1852      6660      2E 40      MVI  L,CNTL      ;RESET BUFFER AODR
1853      6662      36 10      MVI  M,RSTBUF
1854      6664      0E 0F      MVI  C,17Q
1855      6666      AF          XRA  A          ;CLEAR RAM BUFFER
1856      6667      TST710 EQU  S
1857      6667      2E 20      MVI  L,BUFWRT+DATA2
1858      6669      77          MOV  M,A
1859      666A      0D          OCR  C
1860      666B      C2 67 66    JNZ  TST710
1861      666E      2E 04      MVI  L,LPHIR4
1862      6670      36 01      MVI  M,INITFF
1863      6672      2E 01      MVI  L,LPHIR1      ;ENABLE OUT DATA
1864      6674      36 08      MVI  M,OTFIFO
1865      6676      0E 0F      MVI  C,17Q
1866      6678      TST720 EQU  S
1867      6678      2E 00      MVI  L,LPHIRO      ;ROOM AVAILABLE?
1868      667A      7E          MOV  A,M
1869      667B      E6 08      ANI  OTFIFO
1870      667D      CA 78 66    JZ   TST720      ;NO
1871      6680      79          MOV  A,C          ;YES, LAST BYTE?
1872      6681      B7          ORA  A
1873      6682      CA 8C 66    JZ   TST730      ;YES, STORE EOI
1874      6685      2E 02      MVI  L,LPHIR2+DATA2
1875      6687      77          MOV  M,A
1876      6688      0D          DCR  C
1877      6689      C3 78 66    JMP  TST720
1878      ;
1879      668C      TST730 EQU  S
1880      668C      2E 12      MVI  L,LPHIR2+EOI2 ;WRITE EOI
1881      668E      77          MOV  M,A
1882      668F      AF          XRA  A          ;SELECT DMA TO RESPOND
1883      6690      2E 04      MVI  L,LPHIR4      ; TO INPUT REQUESTS
1884      6692      77          MOV  M,A
1885      6693      3E 64      MVI  A,TIMOUT      ;SET UP TIME-OUT
1886      6695      32 79 91    STA  XTIMER
1887      6698      2E 40      MVI  L,CNTL
1888      669A      36 50      MVI  M,RSTOMA+RSTBUF
1889      669C      2E 01      MVI  L,LPHIR1
1890      669E      36 04      MVI  M,INFIFO
1891      66A0      2E 40      MVI  L,CNTL      ;INITIATE PHI TO RAM XFER
1892      66A2      36 08      MVI  M,PHI2BF
1893      66A4      TST740 EQU  S
1894      66A4      2E 40      MVI  L,STAT      ;CHECK FOR COMPLETION
1895      66A6      7E          MOV  A,M
1896      66A7      47          MOV  B,A
1897      66A8      E6 10      ANI  EOIBIT
1898      66AA      C2 BD 66    JNZ  TST750      ;FINISHED
1899      66AD      78          MOV  A,B          ;DMA ACTIVE?
1900      66AE      E6 40      ANI  DMAACT
1901      66B0      CA AF 69    JZ   ERR00      ;NO, ERROR
1902      66B3      3A 79 91    LDA  XTIMER      ;YES, TIME OUT?
=====

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=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                SAMPLE HP-IB DRIVER - 13255-91128      PAGE  48
=====
1903      66B6      B7              ORA      A
1904      66B7      C2 A4 66          JNZ      TST740      ;NO, CONTINUE
1905      66BA      C3 B4 69          JMP      ERR01
1906
1907      66BD              ;
TST750 EQU      $
1908      66BD      2E 41          MVI      L,BUFADR    ;READ BUFFER ADDR
1909      66BF      7E              MOV      A,M
1910      66C0      FE 10          CPI      20Q          ;RIGHT VALUE?
1911      66C2      C2 B9 69          JNZ      ERR02      ;NO
1912      66C5      2E 40          MVI      L,STAT      ;DMA STILL ACTIVE?
1913      66C7      7E              MOV      A,M
1914      66C8      E6 40          ANI      DMAACT
1915      66CA      C2 BE 69          JNZ      ERR03      ;YES
1916      66CD      2E 40          MVI      L,CNTL      ;INITIALIZE BUFFER ADDR
1917      66CF      36 10          MVI      M,RSTBUF
1918      66D1      0E 0F          MVI      C,17Q
1919      66D3              TST760 EQU      $
1920      66D3      2E 20          MVI      L,BUFRD    ;READ THE DATA BYTES
1921      66D5      7E              MOV      A,M
1922      66D6      B9              CMP      C          ;COMPARE WITH WHAT SHOULD
1923      66D7      C2 C3 69          JNZ      ERR04      ;NO, ERROR
1924      66DA      47              MOV      B,A          ;YES, CHECK TYPE OF BYTE
1925      66DB      2E 40          MVI      L,STAT      ;DATA?
1926      66DD      7E              MOV      A,M
1927      66DE      E6 03          ANI      D0+D1
1928      66E0      C2 EA 66          JNZ      TST770      ;NO
1929      66E3      0D              DCR      C          ;YES, PAST LAST BYTE?
1930      66E4      FA C8 69          JM       ERR05      ;YES, ERROR
1931      66E7      C3 D3 66          JMP      TST760      ;NO, CONTINUE READING
1932
1933      66EA              ;
TST770 EQU      $
1934      66EA      FE 03          CPI      IE012      ;EOI BYTE?
1935      66EC      78              MOV      A,B
1936      66ED      C2 CD 69          JNZ      ERR06      ;NO, ERROR
1937      66F0      B7              ORA      A          ;LAST BYTE?
1938      66F1      C2 D2 69          JNZ      ERR07      ;NO,ERROR
=====

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=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                                SAMPLE HP-IB DRIVER - 13255-91128      PAGE  49
=====
1940      ;
1941      ; TEST 8 - WRITE FROM PROCESSOR TO RAM, THEN
1942      ; RAM TO PHI VIA DMA, THEN PHI TO RAM VIA
1943      ; DMA AND FINALLY RAM TO PROCESSOR...
1944      ;
1945      66F4      TST800 EQU $
1946      66F4      3E 38      MVI A,EIGHT
1947      66F6      32 55 FE    STA TESTNO
1948      66F9      2E 40      MVI L,CNTL      ;RESET RAM ADDRESS
1949      66FB      36 10      MVI M,RSTBUF
1950      66FD      3E 0F      MVI A,17B
1951      66FF      TST810 EQU $
1952      66FF      2E 20      MVI L,BUFWRT+DATA2 ;WRITE DATA BYTE
1953      6701      77          MOV M,A
1954      6702      3D          DCR A
1955      6703      C2 FF 66    JNZ TST810
1956      6706      2E B0      MVI L,BUFWRT+EOI2+ENDBIT ;WRITE LAST BYTE
1957      6708      77          MOV M,A
1958      6709      2E 40      MVI L,CNTL      ;RESET RAM ADDR FOR XFER
1959      670B      36 10      MVI M,RSTBUF
1960      670D      2E 04      MVI L,LPHIR4
1961      670F      36 03      MVI M,INITFF+DMASEL
1962      6711      3E 64      MVI A,TIMOUT ;SET UP TIME-OUT
1963      6713      32 79 91    STA XTIMER
1964      6716      2E 40      MVI L,CNTL      ;CLEAR DMA
1965      6718      36 40      MVI M,RSTDMA
1966      671A      2E 01      MVI L,LPHIR1 ;WAIT FOR OUTPUT DATA REQ
1967      671C      36 08      MVI M,DTFIFO
1968      671E      2E 40      MVI L,CNTL      ;INITIATE RAM TO PHI XFER
1969      6720      36 04      MVI M,BF2PHI
1970      6722      TST820 EQU $
1971      6722      2E 40      MVI L,STAT      ;XFER COMPLETED?
1972      6724      7E          MOV A,M
1973      6725      47          MOV B,A
1974      6726      E6 10      ANI EOIBIT
1975      6728      C2 3B 67    JNZ TST830 ;YES
1976      672B      78          MOV A,B ;NO, DMA STILL WORKING?
1977      672C      E6 40      ANI DMAACT
1978      672E      CA AF 69    JZ ERR00 ;NO, ERROR
1979      6731      3A 79 91    LDA XTIMER ;YES, HUNG?
1980      6734      B7          ORA A
1981      6735      C2 22 67    JNZ TST820 ;NO,CONTINUE
1982      6738      C3 B4 69    JMP ERR01
1983      ;
1984      673B      TST830 EQU $
1985      673B      2E 41      MVI L,BUFADR ;XFER COMPLETE, RAM ADDR
1986      673D      7E          MOV A,M
1987      673E      FE 10      CPI 200 ; CORRECT?
1988      6740      C2 B9 69    JNZ ERR02 ;NO
1989      6743      AF          XRA A ;SET DMA SELECT SENSE
1990      6744      2E 04      MVI L,LPHIR4
1991      6746      77          MOV M,A
1992      6747      3E 64      MVI A,TIMOUT
1993      6749      32 79 91    STA XTIMER
1994      674C      2E 40      MVI L,CNTL      ;CLEAR DMA
1995      674E      36 40      MVI M,RSTDMA
1996      6750      2E 01      MVI L,LPHIR1 ;SET FOR RECEIVING DATA

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ITEM	LOC	OBJECT CODE	SOURCE STATEMENTS	SAMPLE HP-IB DRIVER - 13255-91120	PAGE 50
1997	6752	36 04	MVI M,INFIFO		
1998	6754	2E 40	MVI L,CNTL ;XFER FROM PHI TO RAM		
1999	6756	36 08	MVI M,PHI2BF		
2000	6758		TST840 EQU \$		
2001	6758	2E 40	MVI L,STAT ;XFER COMPLETED?		
2002	675A	7E	MOV A,M		
2003	675B	47	MOV B,A		
2004	675C	E6 10	ANI EOIBIT		
2005	675E	C2 71 67	JNZ TST850 ;YES		
2006	6761	78	MOV A,B ;NO, DMA STILL ACTIVE?		
2007	6762	E6 40	ANI DMAACT		
2008	6764	CA BE 69	JZ ERR03 ;NO, ERROR		
2009	6767	3A 79 91	LDA XTIMER ;YES, TIME OUT?		
2010	676A	B7	ORA A		
2011	676B	C2 58 67	JNZ TST840 ;NO, CONTINUE		
2012	676E	C3 C3 69	JMP ERR04		
2013			;		
2014	6771		TST850 EQU \$		
2015	6771	2E 41	MVI L,BUFADR ;IS RAM COUNTER AT CORRECT		
2016	6773	7E	MOV A,M		
2017	6774	FE 20	CPI 40Q ; SPOT?		
2018	6776	C2 C8 69	JNZ ERR05 ;NO		
2019	6779	2E 40	MVI L,STAT ;YES, RESET RAM ADDR		
2020	677B	36 10	MVI M,RSTBUF		
2021	677D	0E 0F	MVI C,17Q		
2022	677F		TST860 EQU \$		
2023	677F	2E 20	MVI L,BUFRD ;READ DATA BYTES THAT WERE		
2024	6781	7E	MOV A,M		
2025			;		
2026	6782	B9	CMP C ; WRITTEN BY PROCESSOR		
2027	6783	C2 CD 69	JNZ ERR06 ;COMPARE WITH WHAT WAS		
2028	6786	0D	DCR C ;NO, ERROR		
2029	6787	F2 7F 67	JP TST860 ;YES, GO TO NEXT BYTE		
2030	678A	0E 0F	MVI C,17Q		
2031	678C		TST870 EQU \$ ;READ BYTES WRITTEN BY DMA		
2032	678C	2E 20	MVI L,BUFRD ;READ BYTE FROM RAM		
2033	678E	7E	MOV A,M		
2034	678F	47	MOV B,A		
2035	6790	2E 40	MVI L,STAT ;GET TYPE OF BYTE		
2036	6792	7E	MOV A,M		
2037	6793	E6 03	ANI D0+D1		
2038	6795	C2 A4 67	JNZ TST880 ;NOT DATA BYTE		
2039	6798	78	MOV A,B ;COMPARE WITH WHAT WAS		
2040	6799	B9	CMP C ; WRITTEN?		
2041	679A	C2 D2 69	JNZ ERR07 ;NO, ERROR		
2042	679D	0D	DCR C ;FINISHED ALL BYTES?		
2043	679E	F2 8C 67	JP TST870 ;NO, CONTINUE		
2044	67A1	C3 D7 69	JMP ERR08		
2045			;		
2046	67A4		TST880 EQU \$		
2047	67A4	FE 03	CPI IE012 ;EOI TYPE OF BYTE?		
2048	67A6	78	MOV A,B		
2049	67A7	C2 DC 69	JNZ ERR09 ;NO, ERROR		
2050	67AA	B7	ORA A ;YES, DID THIS OCCUR WITH		
2051	67AB	C2 E1 69	JNZ ERR10 ;NO, ERROR		

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=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                                SAMPLE HP-IB DRIVER - 13255-91128      PAGE 51
=====
2053                                           ;
2054                                           ; TEST 9 - TEST INTERRUPT CAPABILITIES OF
2055                                           ; HP-IB/PHI PCA, PROCESSOR TO PHI
2056                                           ;
2057      67AE      TST900 EQU $
2058      67AE      MVI A,NINE
2059      67B0      32 55 FE      STA TESTNO
2060      67B3      2E 04      MVI L,LPHIR4
2061      67B5      36 01      MVI M,INITFF
2062      67B7      AF      XRA A
2063      67B8      32 5C FE      STA FLGSV
2064      67BB      32 5B FE      STA FLGSV1
2065      67BE      3A 56 FE      LDA HIBSTT ;SET FOR FAIL INTERRUPT TEST
2066      67C1      E6 FC      ANI 377B-ERRINT-FIN
2067      67C3      F6 01      ORI ERRINT
2068      67C5      32 56 FE      STA HIBSTT
2069      67C8      3E 30      MVI A,600
2070      67CA      32 57 FE      STA HIBERR
2071      67CD      3E 0F      MVI A,170
2072      67CF      32 58 FE      STA HIBCNT ;SET UP WRITE INTERRUPT
2073      67D2      21 29 60      LXI H,WRTINT ; ROUTINE
2074      67D5      22 59 FE      SHLD HIBVEC
2075      67D8      3E 64      MVI A,TIMOUT
2076      67DA      32 79 91      STA XTIMER
2077      67DD      26 88      MVI H,HPIB
2078      67DF      2E 40      MVI L,CNTL ;ENABLE PCA INTERRUPT
2079      67E1      36 20      MVI M,INTENB
2080      67E3      2E 11      MVI L,LPHIR1+PHIINT ;LOOK FOR DATA REQ FROM PHI
2081      67E5      36 08      MVI M,OTFIFO ;VIA OTFIFO INTERRUPTS
2082      67E7      TST910 EQU $
2083      67E7      3A 56 FE      LDA HIBSTT ;INTERRUPT OCCUR ILLEGALLY?
2084      67EA      E6 04      ANI IDLERR
2085      67EC      C2 B4 69      JNZ ERR01 ;YES
2086      67EF      3A 56 FE      LDA HIBSTT ;COMPLETED DATA XFER?
2087      67F2      E6 02      ANI FIN
2088      67F4      C2 01 68      JNZ TST920 ;YES
2089      67F7      3A 79 91      LDA XTIMER ;NO, TIME OUT?
2090      67FA      B7      ORA A
2091      67FB      C2 E7 67      JNZ TST910 ;NO, CONTINUE
2092      67FE      C3 B9 69      JMP ERR02
2093      6801      TST920 EQU $
2094      6801      3A 56 FE      LDA HIBSTT ;DID ERROR OCCUR?
2095      6804      E6 01      ANI ERRINT
2096      6806      CA 10 68      JZ TS1000 ;NO, GO TO NEXT TEST
2097      6809      3A 57 FE      LDA HIBERR ;YES, DISPLAY MESSAGE
2098      680C      47      MOV B,A
2099      680D      C3 53 69      JMP ERRUR2

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=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                                SAMPLE HP-IB DRIVER - 13255-91128      PAGE 52
=====
2101      ;
2102      ; TEST 10 - TEST INTERRUPT CAPABILITIES OF
2103      ; HP-IB/PHI PCA, PHI TO PROCESSOR
2104      ;
2105      6810      TS1000 EQU $
2106      6810      3E 3A      MVI A,TEN
2107      6812      32 55 FE      STA TESTNO
2108      6815      3A 56 FE      LDA HIBSTT
2109      6818      E6 FC      ANI ONES-ERRINT-FIN
2110      681A      F6 01      ORI ERRINT
2111      681C      32 56 FE      STA HIBSTT
2112      681F      3E 30      MVI A,60Q
2113      6821      32 57 FE      STA HIBERR
2114      6824      3E 0F      MVI A,17Q
2115      6826      32 58 FE      STA HIBCNT ;SET UP READ INTERRUPT
2116      6829      21 68 60      LXI H,RDINT ; ROUTINE
2117      682C      22 59 FE      SHLD HIBVEC
2118      682F      3E 64      MVI A,TIMOUT
2119      6831      32 79 91      STA XTIMER
2120      6834      26 88      MVI H,HPIB
2121      6836      2E 11      MVI L,LPHIR1+PHIINT ;ENABLE INTERRUPTS FOR
2122      6838      36 04      MVI M,INFIFO ;INFIFO DATA REQ
2123      683A      TS1010 EQU $
2124      683A      3A 56 FE      LDA HIBSTT ;INTERRUPT OCCURRED WHILE
2125      683D      E6 04      ANI IDLERR ; BETWEEN ROUTINES?
2126      683F      C2 84 69      JNZ ERR01
2127      6842      3A 56 FE      LDA HIBSTT ;COMPLETED DATA XFER?
2128      6845      E6 02      ANI FIN
2129      6847      C2 54 68      JNZ TS1020 ;YES
2130      684A      3A 79 91      LDA XTIMER ;TIME OUT?
2131      684D      B7      ORA A
2132      684E      C2 3A 68      JNZ TS1010 ;NO, CONTINUE
2133      6851      C3 89 69      JMP ERR02
2134      ;
2135      6854      TS1020 EQU $
2136      6854      3A 56 FE      LDA HIBSTT ;ERROR DURING PROCESSING?
2137      6857      E6 01      ANI ERRINT
2138      6859      CA 63 68      JZ TS1100 ;NO
2139      685C      3A 57 FE      LDA HIBERR ;YES, DISPLAY MSG
2140      685F      47      MOV B,A
2141      6860      C3 53 69      JMP ERROR2
=====

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=====				=====	=====	=====
ITEM	LOC	OBJECT CODE	SOURCE STATEMENTS		SAMPLE HP-IB DRIVER - 13255-91128	PAGE 53
=====				=====		
2143			/			
2144			/ TEST 11 - TEST INTERRUPTS FOR THE			
2145			/ DMA MACHINE, CHECK FROM RAM BUFFER			
2146			/ TO PHI AND THEN BACK AGAIN...			
2147			/ THIS TEST DOES IT ALL, RATHER THAN			
2148			/ BREAKING IT UP INTO TWO TESTS...			
2149			/			
2150	6863		TS1100 EQU \$			
2151	6863	3E 3B	MVI A,ELEVEN			
2152	6865	32 55 FE	STA TESTNO			
2153	6868	2E 40	MVI L,CNTL ;RESET ADDR BUF ADDR			
2154	686A	36 10	MVI M,RSTBUF			
2155	686C	3E 0F	MVI A,170			
2156	686E		TS1110 EQU \$			
2157	686E	2E 20	MVI L,BUFWRT+DATA2 ;FILL RAM WITH DATA			
2158	6870	77	MOV M,A			
2159	6871	3D	DCR A			
2160	6872	C2 6E 68	JNZ TS1110			
2161	6875	2E 80	MVI L,BUFWRT+EOI2+ENDBIT			
2162	6877	77	MOV M,A			
2163	6878	AF	XRA A ;CLEAR RAM AREA THAT DMA			
2164	6879	0E 0F	MVI C,17B ; WILL BE WRITING TO			
2165	687B		TS1115 EQU \$			
2166	687B	2E 20	MVI L,BUFWRT+DATA2			
2167	687D	77	MOV M,A			
2168	687E	0D	DCR C			
2169	687F	C2 7B 68	JNZ TS1115			
2170	6882	2E 40	MVI L,CNTL ;RESET RAM BUF ADD			
2171	6884	36 10	MVI M,RSTBUF			
2172	6886	2E 04	MVI L,LPHIR4 ;INIT FIFO'S			
2173	6888	36 03	MVI M,INITFF+DMASEL			
2174	688A	AF	XRA A ;CLEAR FLAGS FOR USE			
2175	688B	32 5C FE	STA FLGSAV ; BY ERROR ROUTINES			
2176	688E	32 5B FE	STA FLGSV1			
2177	6891	3A 56 FE	LDA HIBSTT ;SET ERROR INTERRUPT FLAG			
2178	6894	E6 FC	ANI ONFS-ERRINT-FIN ;IN CASE NOTHING			
2179	6896	F6 01	ORI ERRINT ; HAPPENS			
2180	6898	32 56 FE	STA HIBSTT			
2181	689B	3E 30	MVI A,600			
2182	689D	32 57 FE	STA HIBERR			
2183	68A0	21 A2 60	LXI H,WRTDMA ;SET DMA INTERRUPT ROUTINE			
2184	68A3	22 59 FE	SHLD HIBVEC			
2185	68A6	3E 64	MVI A,TIMOUT			
2186	68A8	32 79 91	STA XTIMER			
2187	68AB	26 88	MVI H,HPIB			
2188	68AD	2E 40	MVI L,CNTL ;CLEAR DMA			
2189	68AF	36 40	MVI M,RSTDMA			
2190	68B1	2E 01	MVI L,LPHIR1 ;ENABLE OUT FIFO DATA FLAG			
2191	68B3	36 08	MVI M,OTFIFO			
2192	68B5	2E 40	MVI L,CNTL ;START XFER			
2193	68B7	36 24	MVI M,BF2PHI+INTENB			
2194	68B9		TS1120 EQU \$			
2195	68B9	3A 56 FE	LDA HIBSTT ;INTERRUPT ERROR?			
2196	68BC	E6 04	ANI IDLERR			
2197	68BE	C2 B4 69	JNZ ERRO1 ;YES			
2198	68C1	3A 56 FE	LDA HIBSTT ;NO, FINISHED XFER?			
2199	68C4	E6 02	ANI FIN			

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=====
ITEM      LOC      OBJECT CODE      SOURCE STATEMENTS      SAMPLE HP-IB DRIVER - 13255-91128      PAGE 54
=====
2200      68C6      C2 D3 68              JNZ TS1130      ;YES
2201      68C9      3A 79 91              LDA XTIMER      ;NO, TIME OUT?
2202      68CC      B7                      ORA A
2203      68CD      C2 B9 68              JNZ TS1120      ;NO
2204      68D0      C3 B9 69              JMP ERROR2
2205      68D3              TS1130 EQU $
2206      68D3      3A 56 FE              LDA HIBSTT      ;ERROR OCCURRED IN
2207      68D6      E6 01              ANI ERRINT      ; INTERRUPT ROUTINE?
2208      68D8      CA E2 68              JZ TS1140      ;NO
2209      68DB      3A 57 FE              LDA HIBERR      ;YES, DISPLAY ERROR MSG
2210      68DE      47                      MOV B,A
2211      68DF      C3 53 69              JMP ERROR2
2212
2213      68E2              TS1140 EQU $
2214      68E2      AF                      XRA A      ;CLEAR ERROR FLAGS
2215      68E3      32 5C FE              STA FLGSAV
2216      68E6      32 5B FE              STA FLGSV1
2217      68E9      3A 56 FE              LDA HIBSTT
2218      68EC      E6 FC              ANI ONES-ERRINT-FIN
2219      68EE      F6 01              ORI ERRINT
2220      68F0      32 56 FE              STA HIBSTT
2221      68F3      3E 33              MVI A,630
2222      68F5      32 57 FE              STA HIBERR      ;SET ERROR FLAG IF NOTHING
2223                      ; HAPPENS
2224      68F8      21 C7 60              LXI H,RDDMA      ;SET DMA READ ROUTINE FOR
2225      68FB      22 59 FE              SHLD HIBVEC      ; INTERRUPT
2226      68FE      3E 64              MVI A,TIMOUT
2227      6900      32 79 91              STA XTIMER
2228      6903      26 88              MVI H,HPIB
2229      6905      AF                      XRA A      ;SET DMA SENSE
2230      6906      2E 04              MVI L,LPHIR4
2231      6908      77                      MOV M,A      ;CLEAR DMA
2232      6909      2E 40              MVI L,CNTL
2233      690B      36 40              MVI M,RSTDMA
2234      690D      2E 01              MVI L,LPHIR1
2235      690F      36 04              MVI M,INFIFO      ;START PHI TO RAM XFER
2236      6911      2E 40              MVI L,CNTL
2237      6913      36 28              MVI M,PHI2BF+INTENB
2238      6915              TS1150 EQU $
2239      6915      3A 56 FE              LDA HIBSTT      ;INTERRUPT ERROR?
2240      6918      E6 04              ANI IDLERR
2241      691A      C2 C3 69              JNZ ERR04      ;YES, REPORT ERROR
2242      691D      3A 56 FE              LDA HIBSTT      ;FINISHED ?
2243      6920      E6 02              ANI FIN
2244      6922      C2 2F 69              JNZ TS1160      ;YES
2245      6925      3A 79 91              LDA XTIMER      ;NO, TIME OUT?
2246      6928      B7                      ORA A
2247      6929      C2 15 69              JNZ TS1150      ;NO
2248      692C      C3 C8 69              JMP ERR05
2249      692F              TS1160 EQU $
2250      692F      3A 56 FE              LDA HIBSTT      ;ERROR IN INTERRUPT
2251      6932      E6 01              ANI ERRINT      ; ROUTINE?
2252      6934      CA 3E 69              JZ ENDTST      ;NO, FINISHED
2253      6937      3A 57 FE              LDA HIBERR      ;YES, DISPLAY ERROR MSG
2254      693A      47                      MOV B,A
2255      693B      C3 53 69              JMP ERROR2
=====

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=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                                     SAMPLE HP-IB DRIVER - 13255-91128      PAGE 55
=====
2257      693E                                     ENDTST EQU  $
2258      693E      AF                                     XRA  A          ;DISABLE INTERRUPTS
2259      693F      32 40 88                               STA  IBCNTL
2260      6942      CD 59 62                               CALL PTPINI
2261
2262                                     ;
2262                                     ; TEST END - DISPLAY TEST OK MESSAGE
2263                                     ;
2264      6945      21 87 69                               LXI  H,TSTMSG   ;SET TEST OK MESSAGE
2265      6948      22 F1 FF                               SHLD MSGPT1
2266      6948      BF                                     CMP  A
2267      694C      CD 40 00                               CALL DSPMSG
2268      694F      C3 EA 62                               JMP  UP
2269
2270                                     ;
2271                                     ;
2271                                     ; ERROR4 - ERROR OCCURED DURING THE PHI REG
2272                                     ; COMPARE OPERATIONS...
2273                                     ;
2274      6952                                     ERROR4 EQU  $
2275      6952      F1                                     POP  PSW
2276
2277                                     ;
2277                                     ; ERROR2 -
2278                                     ;
2279                                     ; ENTRY : B = ERROR NUMBER (ASCII)
2280                                     ;
2281      6953                                     ERROR2 EQU  $
2282      6953      3A 55 FE                               LDA  TESTNO     ;GET TEST NUMBER
2283      6956      32 84 69                               STA  NUMMSG+1   ;STORE IN DISP AREA
2284      6959      78                                     MOV  A,B
2285      695A      32 54 FE                               STA  ERRNO      ;SAVE ERROR NUMBER
2286      695D      32 85 69                               STA  NUMMSG+2   ;STORE IN DISP AREA
2287      6960      21 77 69                               LXI  H,ERRMS2
2288      6963      22 F1 FF                               SHLD MSGPT1
2289      6966      21 83 69                               LXI  H,NUMMSG
2290      6969      22 EF FF                               SHLD MSGPT2
2291      696C      BF                                     CMP  A
2292      696D      CD 40 00                               CALL DSPMSG
2293      6970      3E 46                                     MVI  A,F
2294      6972      32 4F FF                               STA  IOCERR
2295      6975      37                                     STC
2296      6976      C9                                     RET
2297
2298      6977      20 45 52                               ERRMS2 DEF  ' ERROR NO. ',0
2299      6983      20 20 20                               NUMMSG DEF  ' ',EOP
2300      6987      82 20 54                               TSTMSG DEF  INVR,' TEST OK ',EOP
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=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                                SAMPLE HP-IB DRIVER - 13255-91128      PAGE 56
=====
2302      ;
2303      ; WRTREG - WRITE DATA TO PHI REGISTER USING
2304      ; THE TABLE POINTED TO BY D,E
2305      ;
2306      6992      WRTREG EQU $
2307      6992      26 88      MVI H,HPIB
2308      6994      WRG010 EQU $
2309      6994      1A      LDAX D      ;GET REGISTER NUMBER
2310      6995      B7      ORA A      ;FINISHED?
2311      6996      F8      RM      ;YES
2312      6997      6F      MOV L,A
2313      6998      13      INX D
2314      6999      1A      LDAX D      ;GET DATA BYTE
2315      699A      77      MOV M,A      ;STORE IN PHI REG
2316      699B      13      INX D
2317      699C      C3 94 69      JMP WRG010
2318      ;
2319      ; RDREG - READ AND COMPARE DATA THAT EXISTS
2320      ; IN PHI REG WITH THE TABLE VALUE...
2321      ; IF A MISMATCH OCCURS, DO NOT RETURN TO
2322      ; THE CALLER (POP THE RETURN ADDR OFF THE
2323      ; STACK)...
2324      ;
2325      699F      RDREG EQU $
2326      699F      26 88      MVI H,HPIB
2327      69A1      RRG010 EQU $
2328      69A1      1A      LDAX D      ;GET PHI REG NUMBER
2329      69A2      B7      ORA A      ;FINISHED?
2330      69A3      F8      RM      ;YES
2331      69A4      6F      MOV L,A
2332      69A5      13      INX D
2333      69A6      1A      LDAX D      ;GET DATA BYTE
2334      69A7      BE      CMP M      ;COMPARE WITH TABLE VALUE?
2335      69A8      C2 52 69      JNZ ERROR4 ;NO
2336      69AB      13      INX D
2337      69AC      C3 A1 69      JMP RRG010 ;CONTINUE

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ITEM	LOC	OBJECT CODE	SOURCE STATEMENTS	SAMPLE HP-IB DRIVER - 13255-91128	PAGE 57
2339			/		
2340	69AF		ERR00 EQU \$		
2341	69AF	06 30	MVI B,ZERO		
2342	69B1	C3 53 69	JMP ERROR2		
2343			/		
2344	69B4		ERR01 EQU \$		
2345	69B4	06 31	MVI B,ONE		
2346	69B6	C3 53 69	JMP ERROR2		
2347			/		
2348	69B9		ERR02 EQU \$		
2349	69B9	06 32	MVI B,TWO		
2350	69BB	C3 53 69	JMP ERROR2		
2351			/		
2352	69BE		ERR03 EQU \$		
2353	69BE	06 33	MVI B,THREE		
2354	69C0	C3 53 69	JMP ERROR2		
2355			/		
2356	69C3		ERR04 EQU \$		
2357	69C3	06 34	MVI B,FOUR		
2358	69C5	C3 53 69	JMP ERROR2		
2359			/		
2360	69C8		ERR05 EQU \$		
2361	69C8	06 35	MVI B,FIVE		
2362	69CA	C3 53 69	JMP ERROR2		
2363			/		
2364	69CD		ERR06 EQU \$		
2365	69CD	06 36	MVI B,SIX		
2366	69CF	C3 53 69	JMP ERROR2		
2367			/		
2368	69D2		ERR07 EQU \$		
2369	69D2	06 37	MVI B,SEVEN		
2370	69D4	C3 53 69	JMP ERROR2		
2371			/		
2372	69D7		ERR08 EQU \$		
2373	69D7	06 38	MVI B,EIGHT		
2374	69D9	C3 53 69	JMP ERROR2		
2375			/		
2376	69DC		ERR09 EQU \$		
2377	69DC	06 39	MVI B,NINE		
2378	69DE	C3 53 69	JMP ERROR2		
2379			/		
2380	69E1		ERR10 EQU \$		
2381	69E1	06 3A	MVI B,TEN		
2382	69E3	C3 53 69	JMP ERROR2		

```

=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                                SAMPLE HP-IR DRIVER - 13255-9112H      PAGE  58
=====
2384      ;
2385      ;   TSTB02 - POWER CONDITION OF PHI REGISTERS
2386      ;
2387      69E6      TSTB02 EQU $
2388      69E6      00 00      DEF LPHIR0,0
2389      69E8      01 00      DEF LPHIR1,0
2390      69EA      04 00      DEF LPHIR4,0
2391      69EC      05 00      DEF LPHIR5,0
2392      69EE      06 00      DEF LPHIR6,0
2393      69F0      07 00      DEF LPHIR7,0
2394      69F2      80      DEF ENDTBL
2395      ;
2396      ;   TSTB03 - WRITE STUCK DATA BIT PATTERN
2397      ;
2398      69F3      TSTB03 EQU $
2399      69F3      01 AA      DEF LPHIR1,D252
2400      69F5      04 AA      DEF LPHIR4,D252
2401      69F7      05 AA      DEF LPHIR5,D252
2402      69F9      06 AA      DEF LPHIR6,D252
2403      69FB      07 AA      DEF LPHIR7,D252
2404      69FD      80      DEF ENDTBL
2405      ;
2406      ;   TSTB04 - READ STUCK DATA BIT PATTERN
2407      ;
2408      69FE      TSTB04 EQU $
2409      69FE      01 AA      DEF LPHIR1,D252
2410      6A00      04 AA      DEF LPHIR4,D252
2411      6A02      05 AA      DEF LPHIR5,D252
2412      6A04      06 AA      DEF LPHIR6,D252
2413      6A06      07 AA      DEF LPHIR7,D252
2414      6A08      80      DEF ENDTBL
2415      ;
2416      ;   TSTB05 - USE COMPLEMENT OF PREV PATTERN
2417      ;
2418      6A09      TSTB05 EQU $
2419      6A09      01 55      DEF LPHIR1,D125
2420      6A0B      04 55      DEF LPHIR4,D125
2421      6A0D      05 55      DEF LPHIR5,D125
2422      6A0F      06 55      DEF LPHIR6,D125
2423      6A11      07 55      DEF LPHIR7,D125
2424      6A13      80      DEF ENDTBL
2425      ;
2426      ;   TSTB06 - READ COMPLEMENT TEST PATTERN
2427      ;
2428      6A14      TSTB06 EQU $
2429      6A14      01 55      DEF LPHIR1,D125
2430      6A16      04 54      DEF LPHIR4,D125-1Q
2431      6A18      05 55      DEF LPHIR5,D125
2432      6A1A      06 55      DEF LPHIR6,D125
2433      6A1C      07 55      DEF LPHIR7,D125
2434      6A1E      80      DEF ENDTBL

```

```

=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS
=====
2436                                     ;
2437                                     ; TSTB07 - STORE PHI REGISTER NUMBER
2438                                     ;
2439      6A1F                                     TSTB07 EQU $
2440      6A1F      01 01                      DEF LPHIR1,1
2441      6A21      04 04                      DEF LPHIR4,4
2442      6A23      05 05                      DEF LPHIR5,5
2443      6A25      06 06                      DEF LPHIR6,6
2444      6A27      07 07                      DEF LPHIR7,7
2445      6A29      80                          DEF ENDTBL
2446                                     ;
2447                                     ; TSTB08 - READ PHI REGISTER NUMBER
2448                                     ;
2449      6A2A                                     TSTB08 EQU $
2450      6A2A      01 01                      DEF LPHIR1,1
2451      6A2C      04 04                      DEF LPHIR4,4
2452      6A2E      05 05                      DEF LPHIR5,5
2453      6A30      06 06                      DEF LPHIR6,6
2454      6A32      07 07                      DEF LPHIR7,7
2455      6A34      80                          DEF ENDTBL
=====

```

```

=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                                SAMPLE HP-IB DRIVER - 13255-91128      PAGE 60
=====
2457      ;
2458      ;      BF2PTP - OUTPUT RECORD TO HP-IB DEVICE
2459      ;
2460      ;      ENTRY : ADRLIS = DEVICE ADDRESS
2461      ;      D,E -> BUFFER STATUS
2462      ;
2463      ;      EXIT : A,B,C,H,L DESTROYED
2464      ;      NC => SUCCESS
2465      ;      D,E -> BUFFER STATUS
2466      ;      IOCERR = S
2467      ;      C => NO HP-IB RESPONSE
2468      ;      IOCERR = F
2469      ;      MSGPT1 -> MESSAGE
2470      ;
2471      6A35      BF2PTP EQU $
2472      6A35      3A 78 91      LDA ADRLIS
2473      6A38      32 72 91      STA IBADR2
2474      6A3B      3A 77 91      LDA LISSEC
2475      6A3E      32 71 91      STA SECNDY
2476      6A41      CD 7A 6F      CALL GETPTR      ;GET DATA POINTER
2477      6A44      1B      DCX D
2478      6A45      1A      LDAX D      ;GET TYPE OF BUFFER
2479      6A46      B7      ORA A
2480      6A47      F2 63 6A      JP B2P080      ;NOT DATA
2481      6A4A      22 6F 91      SHLD BFADR2      ;SAVE ADDRESS
2482      6A4D      1B      DCX D
2483      6A4E      1A      LDAX D
2484      6A4F      32 6E 91      STA BFLEN2      ;GET DATA LENGTH
2485      6A52      3A 7A 91      LDA ADDRST
2486      6A55      E6 80      ANI FCSW
2487      6A57      32 6D 91      STA FLAGS2
2488      6A5A      D5      PUSH D
2489      6A5B      CD A6 6C      CALL HPIBWR      ;WRITE THE RECORD
2490      6A5E      D1      POP D
2491      6A5F      DA 6B 6A      JC B2P200      ;ERROR OCCURRED
2492      6A62      13      INX D
2493      6A63      B2P080 EQU $
2494      6A63      13      INX D
2495      6A64      1A      LDAX D
2496      6A65      E6 EF      ANI ONES-ALTIO
2497      6A67      12      STAX D
2498      6A68      C3 EA 62      JMP UP

```

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=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                                SAMPLE HP-IB DRIVER - 13255-9112#      PAGE 61
=====
2500      ;
2501      ; SET UP ERROR RETURN, I/O SYS CLEARS BUFFERS
2502      ;
2503      6A6B      B2P200 EQU $
2504      6A6B      3A 04 88      LDA PHIRG4      ;CLEAR OUT FIFO OF DATA
2505      6A6E      F6 01      ORI INITFF
2506      6A70      32 04 88      STA PHIRG4
2507      6A73      3E 01      MVI A,FREEZE      ;CLEAR OUT FREEZE, IF ANY
2508      6A75      32 03 88      STA PHIRG3
2509      6A78      3E 40      MVI A,RSTDMA      ;CLEAR DMA, IF NEEDED
2510      6A7A      32 40 88      STA IBCNTL
2511      6A7D      CD 1A 6F      CALL UNLIST      ;UNLISTEN HP-IB DEVICES
2512      6A80      DOWN EQU $
2513      6A80      21 8D 6A      LXI H,NOPNCH
2514      6A83      22 F1 FF      SHLD MSGPT1
2515      6A86      3E 46      MVI A,F
2516      6A88      32 4F FF      STA IOCERR
2517      6A8B      37      STC
2518      6A8C      C9      RET
2519      6A8D      82 20 48      NOPNCH DEF INVR,' HP-IB DOWN ',EOP
=====

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=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                                SAMPLE HP-IB DRIVER - 13255-91128      PAGE  62
=====
2521      ;
2522      ; PTP2BF - READ A RECORD FROM HP-IB DEVICE
2523      ;
2524      ; ENTRY : ADRTLK = DEVICE ADDRESS
2525      ;
2526      ; EXIT : A,B,C,H,L DESTROYED
2527      ; NC => SUCCESSFUL READ
2528      ; D,E -> BUFFER STATUS
2529      ; C => ERROR
2530      ; IOCERR = U => USER INTERRUPT
2531      ; IOCERR = F => NO DATA
2532      ; MSGPT1 -> ERROR MESSAGE
2533      ; D,E -> BUFFER STATUS
2534      ;
2535      6A9B      PTP2BF EQU S
2536      6A9B      3A 76 91      LDA ADRTLK
2537      6A9E      32 72 91      STA IBADR2
2538      6AA1      3A 75 91      LDA TLKSEC
2539      6AA4      32 71 91      STA SECNDY
2540      6AA7      P2B010 EQU S
2541      6AA7      CD 85 6F      CALL RETSCN ;USFR INTERRUPT?
2542      6AAA      D8 ;YES
2543      6AAB      11 3A FF      LXI D,B1STAT ;NO, BUFFER 1 FREE?
2544      6AAE      1A      LDAX D
2545      6AAF      B7      ORA A
2546      6AB0      CA 8B 6A      JZ P2B020 ;YES
2547      6AB3      11 37 FF      LXI D,B2STAT ;NO, BUFFER 2 FREE?
2548      6AB6      1A      LDAX D
2549      6AB7      B7      ORA A
2550      6AB8      C2 A7 6A      JNZ P2B010 ;NO, CONTINUE WAITING FOR BUFFER
2551      6ABB      P2B020 EQU S
2552      6ABB      3E 10      MVI A,ALTIO ;MARK BUFFER BUSY
2553      6ABD      12      STAX D
2554      6ABE      CD 7A 6F      CALL GETPTR ;GET DATA POINTER
2555      6AC1      22 6F 91      SHLD BFADR2
2556      6AC4      AF      XRA A
2557      6AC5      32 6E 91      STA BFLEN2 ;SET UP EXPECTED BUFFER LENGTH
2558      6AC8      3A 7A 91      LDA ADDRST ;CHECK FOR DMA TYPE INPUT
2559      6ACB      E6 80      ANI FCSW
2560      6ACD      F6 01      ORI LFDET
2561      6ACF      32 6D 91      STA FLAGS2
2562      6AD2      D5      PUSH D
2563      6AD3      CD 67 6D      CALL HP1BRD ;READ A RECORD
2564      6AD6      D1      POP D
2565      6AD7      DA E8 6A      JC P2B200
2566      6ADA      1B      DCX D
2567      6ADB      3E FF      MVI A,-1 ;SET BUFFER TYPE TO DATA
2568      6ADD      12      STAX D
2569      6ADE      1B      DCX D
2570      6ADF      3A 6E 91      LDA BFLEN2 ;SAVE BUFFER LENGTH
2571      6AE2      12      STAX D
2572      6AE3      13      INX D
2573      6AE4      13      INX D
2574      6AE5      C3 EA 62      JMP UP
=====

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=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                                SAMPLE HP-IB DRIVER - 13255-91128      PAGE  63
=====
2576                                     ;
2577                                     ; IF ERROR OCCURRED, RETURN END OF FILE
2578                                     ;
2579      6AE8                                     P2B200 EQU $
2580      6AE8      3A 04 88                      LDA PHIRG4      ;CLEAR OUT FIFO OF DATA
2581      6AEB      F6 01                        ORI INITFF
2582      6AED      32 04 88                      STA PHIRG4
2583      6AF0      3E 01                        MVI A,FREEZE      ;CLEAR OUT FREEZE, IF ANY
2584      6AF2      32 03 88                      STA PHIRG3
2585      6AF5      3E 40                        MVI A,RSTDMA     ;CLEAR DMA, IF NEEDED
2586      6AF7      32 40 88                      STA IBCNTL
2587      6AFA      CD 43 6F                      CALL TERMTK      ;RETURN TALK FUNCTION TO TERMINAL
2588      6AFD      CD 1A 6F                      CALL UNLIST      ;UNLISTEN HP-IB DEVICES
2589      6B00      1B                             DCX D
2590      6B01      3E 01                        MVI A,1          ;SET FOR END OF FILE
2591      6B03      12                             STAX D
2592      6B04      1B                             DCX D
2593      6B05      97                             SUB A
2594      6B06      12                             STAX D
2595      6B07      13                             INX D
2596      6B08      13                             INX D
2597      6B09      C3 EA 62                      JMP UP
=====

```



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=====
ITEM    LOC    OBJECT CODE    SOURCE STATEMENTS                                SAMPLE HP-IB DRIVER - 13255-91126    PAGE 64
=====
2599                                          ;
2600                                          ; LSTN00 = SPECIFY LISTEN ADDR
2601                                          ; IF NEGATIVE NUMBER, SPECIFY LISTEN SECONDARY
2602                                          ;
2603                                          ; ENTRY : IOCCNT = HP-IB ADDRESS OF DEVICE
2604                                          ;
2605      6B0C                                LSTN00 EQU $
2606      6B0C      3A DC FF                    LDA IOPSGN      ;NEGATIVE NUMBER?
2607      6B0F      87                        ADD A
2608      6B10      FA 28 6B                    JM LST040      ;YES, SET UP SECONDARY
2609      6B13      3A D6 FF                    LDA IOCCNT+1    ;NUMBER > 30?
2610      6B16      B7                        ORA A
2611      6B17      C2 22 6B                    JNZ LST010     ;YES, RESET ADDRESS TO 30
2612      6B1A      3A D5 FF                    LDA IOCCNT
2613      6B1D                                LST005 EQU $
2614      6B1D      FE 1E                        CPI TERMID
2615      6B1F      DA 24 6B                    JC LST020      ;NO
2616      6B22                                LST010 EQU $
2617      6B22      3E 1E                        MVI A,TERMID
2618      6B24                                LST020 EQU $
2619      6B24      32 78 91                    STA ADRLIS     ;STORE HP-IB ADDRESS
2620      6B27      C9                        RET
2621                                          ;
2622      6B28                                LST040 EQU $
2623      6B28      3A D6 FF                    LDA IOCCNT+1    ;SECONDARY > 31?
2624      6B2B      B7                        ORA A
2625      6B2C      C2 37 6B                    JNZ LST050     ;YES, RESET TO NO SECONDARY
2626      6B2F      3A D5 FF                    LDA IOCCNT
2627      6B32      FE 20                        CPI MAXADR
2628      6B34      DA 39 6B                    JC LST060      ;NO
2629      6B37                                LST050 EQU $
2630      6B37      3E 80                        MVI A,NOSEC
2631      6B39                                LST060 EQU $
2632      6B39      32 77 91                    STA LISSEC     ;STORE SECONDARY ADDRESS
2633      6B3C      C9                        RET

```

```

=====
ITEM    LOC    OBJECT CODE  SOURCE STATEMENTS                                SAMPLE HP-IB DRIVER - 13255-91128    PAGE 65
=====
2635                                          ;
2636                                          ;  TLKR00 - SET UP NEW TALKER ADDRESS
2637                                          ;    AND IF 30 OR GREATER, SET TO 30...
2638                                          ;
2639                                          ;    A NEGATIVE NUMBER INDICATES A
2640                                          ;    SECONDARY COMMAND AND IF LESS THAN
2641                                          ;    -32 THEN THE SECONDARY COMMAND IS
2642                                          ;    NULLIFIED BY SETTING THE MSB TO 1...
2643                                          ;
2644                                          ;    ENTRY : IOCCNT = NEW ADDRESS OF HP-IB
2645                                          ;            TALKER
2646                                          ;
2647      6B3D      TLKR00 EQU $
2648      6B3D      3A DC FF      LDA  IOPSGN
2649      6B40      87              ADD  A
2650      6B41      FA 59 6B      JM   TLKR40
2651      6B44      3A D6 FF      LDA  IOCCNT+1 ;BYTE <> 0?
2652      6B47      B7              ORA  A
2653      6B48      C2 53 6B      JNZ  TLKR10 ;YES, NUMBER TOO BIG
2654      6B4B      3A D5 FF      LDA  IOCCNT ;NO, BYTE >= 30 ?
2655                                          ;
2656                                          ;  ALTERNATE ENTRY POINT
2657                                          ;
2658      6B4E      TLKR05 EQU $
2659      6B4E      FE 1E          CPI  TERMID
2660      6B50      DA 55 6B      JC   TLKR20 ;NO, STORE NEW TALK ADDR
2661      6B53      TLKR10 EQU $
2662      6B53      3E 1E          MVI  A,TERMID ;SET DEFAULT TALK ADDR
2663      6B55      TLKR20 EQU $
2664      6B55      32 76 91      STA  ADRTLK
2665      6B58      C9              RET
2666                                          ;
2667      6B59      TLKR40 EQU $
2668      6B59      3A D6 FF      LDA  IOCCNT+1 ;SECONDARY > 32?
2669      6B5C      B7              ORA  A
2670      6B5D      C2 68 6B      JNZ  TLKR50 ;YES
2671      6B60      3A D5 FF      LDA  IOCCNT
2672      6B63      FE 20          CPI  MAXADR
2673      6B65      DA 6A 6B      JC   TLKR60 ;NO
2674      6B68      TLKR50 EQU $
2675      6B68      3E 80          MVI  A,NOSEC
2676      6B6A      TLKR60 EQU $
2677      6B6A      32 75 91      STA  TLKSEC ;SAVE SECONDARY ADDRESS
2678      6B6D      C9              RET

```

```

=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                                SAMPLE HP-IB DRIVER - 13255-91128      PAGE 66
=====
2680      ;
2681      ; CHARIN - CHARACTER MODE OPERATION FOR
2682      ; HP-IB DEVICE...ALLOWS TERMINAL TO BE
2683      ; USED AS NORMAL LISTENER/TALKER WITHOUT
2684      ; CONTROL CAPABILITIES...
2685      ;
2686      ;   ACCESSED THRU SCNVEC...
2687      ;
2688      6B6E      CHARIN EQU $
2689      6B6E      CHRI00 EQU $
2690      6B6E      3A 03 88      LDA PHIRG3      ;CONTROLLER IN CHARGE?
2691      6B71      E6 10      ANI CIC
2692      6B73      C2 FA 6B      JNZ CHECK      ;YES, I DETERMINE WHO RCV/SEND DATA
2693      6B76      3A 00 88      LDA PHIRG0
2694      6B79      E6 04      ANI INFIFO
2695      6B7B      CA A0 6B      JZ CHRI30      ;NO, CHECK FOR OUT REQ
2696      6B7E      CHRI15 EQU $
2697      6B7E      3A 02 88      LDA PHIRG2
2698      6B81      E6 7F      ANI 177Q
2699      6B83      4F      MOV C,A
2700      6B84      CD 82 00      CALL CHINT      ;SEND TO DISPLAY
2701      6B87      CA 6E 6B      JZ CHARIN
2702      6B8A      CHRI20 EQU $
2703      6B8A      3A C0 FF      LDA CURROW
2704      6B8D      32 20 87      STA IOCRRW
2705      6B90      FB      EI
2706      6B91      3E 02      MVI A,RSTON
2707      6B93      32 80 83      STA IOKBCO
2708      6B96      BF      CMP A
2709      6B97      3A C1 FF      LDA CURCOL
2710      6B9A      32 00 87      STA IOCRCL
2711      6B9D      C3 6E 6B      JMP CHARIN

```

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=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                                SAMPLE HP-IB DRIVER - 13255-91128      PAGE 67
=====
2713      ;
2714      ; CHECK IF I NEED TO SEND DATA
2715      ;
2716      6BA0      CHRI30 EQU $
2717      6BA0      3A 00 88      LDA PHIRGO
2718      6BA3      E6 08      ANI OTFIFO
2719      6BA5      C8      RZ      ;NO
2720      6BA6      3A 03 88      LDA PHIRG3      ;YES, IS PHI TALKER?
2721      6BA9      E6 04      ANI P3TALK
2722      6BA8      C8      RZ      ;NO, RETURN
2723      6BAC      3A 04 88      LDA PHIRG4      ;CLEAR OUT FIFO OF DATA
2724      6BAF      F6 01      ORI INITFF
2725      6BB1      32 04 88      STA PHIRG4
2726      6BB4      3E 01      MVI A,FREEZE
2727      6BB6      32 03 88      STA PHIRG3      ;UNFREEZE OUTBOUND FIFO
2728      6BB9      CHRI50 EQU $
2729      6BB9      CD 05 48      CALL ZGETKY      ;YES, ANY KEYBOARD INPUT?
2730      6BBC      C2 6E 68      JNZ CHARIN      ;NO, WAIT UNTIL KEY IS PRESSED
2731      6BBF      B7      ORA A      ;SPECIAL KEYS?
2732      6BC0      FA D3 6B      JM CHR200      ;YES
2733      6BC3      E6 7F      ANI 177Q
2734      6BC5      4F      MOV C,A
2735      6BC6      CD 66 6E      CALL DATAOT
2736      6BC9      D8      RC
2737      6BCA      CD 82 00      CALL CHINT      ;DISPLAY THE CHARACTER
2738      6BCD      CA 6E 6B      JZ CHARIN
2739      6BD0      C3 8A 68      JMP CHRI20
2740      ;
2741      6BD3      CHR200 EQU $
2742      6BD3      FE A1      CPI 241Q      ;FUNCTION KEYS?
2743      6BD5      FA 6E 6B      JM CHARIN      ;YES, IGNORE
2744      6BD8      FE F0      CPI 360Q      ;F1 THRU F8?
2745      6BDA      DA E2 6B      JC CHR210      ;NO, HANDLE ESC SEQ
2746      6BDD      FE F8      CPI 370Q      ;F1 THRU F8?
2747      6BDF      DA 6E 6B      JC CHARIN      ;YES, IGNORE
2748      6BE2      CHR210 EQU $
2749      6BE2      32 55 FF      STA TESTNO
2750      6BE5      3E 1B      MVI A,ESC      ;SET UP ESC SEQ FOR 'CHINT'
2751      6BE7      4F      MOV C,A
2752      6BE8      CD 82 00      CALL CHINT
2753      6BE8      3A 55 FE      LDA TESTNO
2754      6BEE      E6 7F      ANI 177Q
2755      6BF0      4F      MOV C,A
2756      6BF1      CD 82 00      CALL CHINT
2757      6BF4      CA 6E 6B      JZ CHARIN
2758      6BF7      C3 8A 68      JMP CHRI20

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=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                                SAMPLE HP-IB DRIVER - 13255-91128      PAGE 68
=====
2760      ;
2761      ; CHECK - DETERMINE IF ANY DEVICE IS ASSERTING
2762      ; SRQ OR PARALLEL POLL
2763      ;
2764      6BFA      CHECK EQU $
2765      6BFA      3A 00 88      LDA PHIRGO      ;PARALLEL POLL AVAILABLE?
2766      6BFD      E6 20      ANI PPIN
2767      6BFF      C2 88 6C      JNZ CHK100      ;YES, CHECK FURTHER
2768      6C02      3A 00 88      LDA PHIRGO      ;SERIAL POLL AVAILABLE?
2769      6C05      E6 10      ANI SRQIN
2770      6C07      C8      RZ      ;NO
2771      ;
2772      ; DO A SERIAL POLL OF THE DEVICES THAT ARE LISTED
2773      ; IN SRQTBL AND PLACE THE ADDRESS OF THE FIRST DNE
2774      ; THAT RESPONDS AFFIRMATIVELY IN 'SRQADR'; IF NONE
2775      ; RESPOND THEN PUT 31 IN 'SRQADR'...
2776      ;
2777      6C08      3E 1F      MVI A,31
2778      6C0A      32 62 FE      STA SRQADR
2779      6C0D      3E 18      MVI A,SPE      ;START SERIAL POLL MODE
2780      6C0F      CD 0C 6F      CALL COMMND
2781      6C12      21 64 FE      LXI H,SRQTBL      ;INITIALIZE TABLE LDOKUP
2782      6C15      1E 04      MVI E,4      ;E = NO. OF ENTRIES
2783      6C17      06 00      MVI B,0      ;B = MULTIPLE OF 8 FOR EACH ENTRY
2784      6C19      SRQX10 EQU $
2785      6C19      0E 00      MVI C,0      ;C = BIT NO. THAT IS SET
2786      6C1B      7E      MOV A,M
2787      6C1C      SRQX20 EQU $
2788      6C1C      0F      RRC
2789      6C1D      DA 3E 6C      JC SRQX40
2790      6C20      SRQX30 EQU $
2791      6C20      0C      INR C
2792      6C21      57      MOV D,A
2793      6C22      79      MOV A,C
2794      6C23      FE 08      CPI 8
2795      6C25      7A      MOV A,D
2796      6C26      C2 1C 6C      JNZ SRQX20
2797      6C29      3E 08      MVI A,8
2798      6C2B      80      ADD B
2799      6C2C      47      MOV B,A
2800      6C2D      23      INX H
2801      6C2E      1D      DCR E
2802      6C2F      C2 19 6C      JNZ SRQX10
2803      6C32      SRQX35 EQU $
2804      6C32      3E 19      MVI A,SPD      ;REMDVE SERIAL POLL MDDE
2805      6C34      CD 0C 6F      CALL COMMND
2806      6C37      CD 43 6F      CALL TERMTK
2807      6C3A      D4 1A 6F      CNC UNLIST
2808      6C3D      C9      RET
2809      ;
2810      6C3E      SRQX40 EQU $
2811      6C3E      79      MOV A,C      ;GET SERIAL POLL RESPONSE
2812      6C3F      80      ADD B
2813      6C40      F5      PUSH PSW
2814      6C41      C5      PUSH B
2815      6C42      CD 45 6F      CALL TLK010
2816      6C45      D4 1F 6F      CNC TERMLS
=====

```

```

=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                                SAMPLE HP-IB DRIVER - 13255-91128      PAGE 69
=====
2817      6C48                      SRQX50 EQU $
2818      6C48      3A 00 88          LDA PHIRGO      ;BE SURE THE TALK AND LISTEN ADDRESSES
2819      6C4B      E6 02                      ANI OTFEMP      ; HAVE BEEN RECEIVED BEFORE READING SRQ BYTE
2820      6C4D      CA 48 6C          JZ SRQX50
2821      6C50      3E 01                      MVI A,1        ;SET TO INPUT 1 CHAR
2822      6C52      CD CC 6E          CALL PCT005
2823      6C55      3E 64                      MVI A,TIMOUT
2824      6C57      32 79 91          STA XTIMER
2825      6C5A                      SRQX55 EQU $
2826      6C5A      3A 00 88          LDA PHIRGO      ;ANY DATA BYTE?
2827      6C5D      E6 04                      ANI INFIFO
2828      6C5F      CA 6E 6C          JZ SRQX60      ;NO, DEVICE IS NOT AVAILABLE
2829      6C62      3A 02 88          LDA PHIRG2      ;YES, IS IT REQUESTING SERVICE?
2830      6C65      47                      MOV B,A
2831      6C66      E6 40                      ANI SRQMSK
2832      6C68      C2 7D 6C          JNZ SRQX70      ;YES, SAVE INFO ABOUT THIS
2833      6C6B      C3 75 6C          JMP SRQX65
2834      6C6E                      SRQX60 EQU $
2835      6C6E      3A 79 91          LDA XTIMER      ;TIME OUT FOR SRQ BYTE?
2836      6C71      B7                      ORA A
2837      6C72      C2 5A 6C          JNZ SRQX55      ;NO, CONTINUE WAITING
2838      6C75                      SRQX65 EQU $
2839      6C75      CD F8 6E          CALL INITPH      ;NO, CLEAR THE FIFO'S AND GOTO NEXT ADDR
2840      6C78      C1                      POP B
2841      6C79      F1                      POP PSW
2842      6C7A      C3 20 6C          JMP SRQX30
2843                      ;
2844      6C7D                      SRQX70 EQU $
2845      6C7D      78                      MOV A,B        ;STORE THE STATUS
2846      6C7E      32 5F FE          STA SRQSTA
2847      6C81      C1                      POP B
2848      6C82      F1                      POP PSW
2849      6C93      F6 80                      ORI 200Q
2850      6C85      32 62 FE          STA SRQADR      ;STORE THE DEVICE ADDR THAT ANSWERED
2851      6C88      C3 32 6C          JMP SRQX35
2852                      ;
2853                      ;
2854      6C8B                      CHK100 EQU $
2855      6C8B      3A 02 88          LDA PHIRG2      ;READ PARALLEL POLL STATUS
2856      6C8E      47                      MOV B,A
2857      6C8F      3A 63 FE          LDA PPBYTE      ;ANY MATCHES WITH WHAT USER WANTS?
2858      6C92      A0                      ANA B
2859      6C93      B7                      ORA A
2860      6C94      C8                      RZ
2861      6C95      32 61 FE          STA PPADR      ;YES, SAVE THE BITS
2862      6C98      3A 74 91          LDA IBFLGS
2863      6C9B      F6 04                      ORI PPRES
2864      6C9D      32 74 91          STA IBFLGS
2865      6CA0      C9                      RET
=====

```

```

=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                                SAMPLE HP-IB DRIVER - 13255-91128      PAGE  70
=====
2867                                           ;
2868                                           ; * * * * *
2869                                           ;
2870                                           ;       PTPMON - DECREMENT TIMING COUNTER
2871                                           ;
2872                                           ;       ENTRY:  DON'T CARE
2873                                           ;
2874                                           ;       EXIT :   TIMER DECREMENTED
2875                                           ;
2876                                           ;
2877      6CA1                                           PTPMON EQU  $
2878      6CA1      21 79 91      LXI  H,XTIMER  ; DECREMENT TIME-OUT COUNTER
2879      6CA4      35              DCR  M
2880      6CA5      C9              RET

```

```

=====
ITEM      LDC   OBJECT CDDE  SOURCE STATEMENTS                                     SAMPLE HP-IB DRIVER - 13255-91128      PAGE  71
=====
2882      ;
2883      ; HPIBWR - HP-IB WRITE DRIVER
2884      ;
2885      ; ENTRY : DATA AREA 2 HAS BEEN SET UP AS FOLLOWS
2886      ;
2887      ; IBADR2 = HP-IB ADDR OF DEVICE RECEIVING DATA
2888      ; SECNDY = SECNDARY ADDRESS FOR DEVICE, IF ANY
2889      ; ( 200B => NO SECONDARY )
2890      ; BFADR2 = PTR TO FIRST BYTE OF DATA
2891      ; BFLEN2 = DATA LENGTH
2892      ; FLAGS2 = ENABLE APPROPRIATE MODES
2893      ;
2894      ; EXIT : NC => NO ERROR OCCURRED
2895      ; A,R,D,E,H,L DESTROYED
2896      ; STRT2 = 0
2897      ;
2898      ; C => ERROR OCCURRED
2899      ; A,R,D,E,H,L DESTROYED
2900      ; STRT2 = ERROR CODE
2901      ;
2902      ;
2903      6CA6      HPIBWR EQU S
2904      6CA6      CD E8 6E      CALL CNTLR ;CONTROLLER-IN-CHARGE?
2905      6CA9      DA DC 6C      JC HPW020 ;NO,
2906      6CAC      D4 1A 6F      CNC UNLIST ;UNLISTEN ALL DEVICES
2907      6CAF      D4 43 6F      CNC TERMTK ;YES, SET UP TERMINAL TO TALK
2908      6CB2      D4 14 6F      CNC LISTEN ;THEN SET UP LISTENER
2909      6CB5      D4 2B 6F      CNC SECNDN ; THEN SET UP SECNDARY
2910      6CB8      D8          RC ;ND, ERROR SOMEWHERE ALDNG THE SETUP
2911      ;
2912      6CB9      2A 6F 91      LHLD BFADR2 ;GET DATA BUFFER POINTER
2913      6CBC      3A 6E 91      LDA BFLEN2 ;GET BUFFER LENGTH
2914      6CBF      5F          MOV E,A
2915      6CC0      3A 6D 91      LDA FLAGS2
2916      6CC3      E6 80      ANI DMA
2917      6CC5      C2 12 6D      JNZ HPW100
2918      6CC8      HPW005 EQU S
2919      6CC8      7E          MOV A,M ;GET DATA BYTE FROM BUFFER
2920      6CC9      1D          DCR E ;LAST BYTE?
2921      6CCA      CA D5 6C      JZ HPW010 ;YES
2922      6CCD      CD 66 6E      CALL DATAOT ;NO, OUTPUT THE BYTE
2923      6CD0      D8          RC
2924      6CD1      23          INX H
2925      6CD2      C3 C8 6C      JMP HPW005
2926      ;
2927      6CD5      HPW010 EQU S
2928      6CD5      CD 8A 6E      CALL EOIDUT ;OUTPUT THE BYTE WITH EOI
2929      6CD8      D4 1A 6F      CNC UNLIST ;UNLISTEN THE DEVICE
2930      6CDB      C9          RET

```



```

=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                                SAMPLE HP-IB DRIVER - 13255-91128                                PAGE 72
=====
2932                                           ;
2933                                           ; NON-CONTROLLER OUTPUT IS REQUESTED
2934                                           ; JUST SEND THE DATA WITHOUT ANY HP-IB ADDRESSING
2935                                           ;
2936      6CDC                                           HPW020 EQU $
2937      6CDC      3A 74 91      LDA IBFLGS      ;WAS NON-CONTROLLER MODE ENABLED?
2938      6CDF      E6 02      ANI NCM
2939      6CE1      CA F0 6E      JZ CTL010      ;NO, ERROR
2940      6CE4      3A 00 88      LDA PHIRG0      ;VERIFY THE INPUT FIFO IS EMPTY
2941      6CE7      E6 04      ANI INFIFO      ; SO OUTPUT FIFO CAN BE UNFROZEN
2942      6CE9      CA F2 6C      JZ HPW022
2943      6CEC      3A 02 88      LDA PHIRG2      ;GET BYTE FROM INPUT FIFO
2944      6CEF      C3 DC 6C      JMP HPW020      ;CHECK FOR MORE
2945                                           ;
2946      6CF2                                           HPW022 EQU $
2947      6CF2      3E 01      MVI A,FREEZE      ;UNFREEZE OUTPUT FIFO
2948      6CF4      32 03 88      STA PHIRG3
2949                                           ;
2950      6CF7      2A 6F 91      LHLD BFADR2      ;GET DATA BUFFER POINTER
2951      6CFA      3A 6E 91      LDA BFLEN2      ;GET BUFFER LENGTH
2952      6CFD      5F      MOV E,A
2953      6CFE      3A 6D 91      LDA FLAGS2
2954      6D01                                           HPW025 EQU $
2955      6D01      7E      MOV A,M
2956      6D02      1D      DCR E
2957      6D03      CA 0E 6D      JZ HPW030
2958      6D06      CD 66 6E      CALL DATAOT
2959      6D09      D8      RC
2960      6D0A      23      INX H
2961      6D0B      C3 01 6D      JMP HPW025
2962                                           ;
2963      6D0E                                           HPW030 EQU $
2964      6D0E      CD 8A 6E      CALL EOIOUT
2965      6D11      C9      RET
=====

```

```

=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                                SAMPLE HP-IB DRIVER - 13255-91128      PAGE 73
=====
2967      ;
2968      ; DMA OUTPUT IS REQUESTED
2969      ;
2970      6012      HPW100 EQU $
2971      6012      3A 73 91      LDA CNTLWD      ;RESET RAM BUFFER ADDRESS POINTER
2972      6015      F6 10      ORI RSTBUF
2973      6017      32 40 88      STA IBCNTL
2974      6D1A      HPW110 EQU $
2975      601A      7E      MOV A,M      ;WRITE DATA FROM I/O BUFFER TO
2976      6D1B      1D      DCR E      ; DMA RAM FIFO
2977      601C      CA 26 6D      JZ HPW120
2978      601F      32 20 88      STA IBBFWR+DATA2
2979      6D22      23      INX H
2980      6D23      C3 1A 6D      JMP HPW110
2981      ;
2982      6026      HPW120 EQU $
2983      6026      32 B0 88      STA IBBFWR+EOI2+ENOBIT
2984      6D29      3A 73 91      LDA CNTLWD      ;RESET RAM BUFFER POINTER
2985      602C      F6 10      ORI RSTBUF
2986      602E      32 40 88      STA IBCNTL
2987      6031      3A 04 88      LOA PHIRG4      ;SET UP DMA SENSE DIRECTION
2988      6034      F6 02      ORI DMASEL
2989      6D36      32 04 88      STA PHIRG4
2990      6D39      0E 00      MVI C,0
2991      603B      3A 73 91      LOA CNTLWD      ;START DMA TRANSFER
2992      6D3E      F6 04      ORI BF2PHI
2993      6D40      32 40 88      STA IBCNTL
2994      6043      HPW125 EQU $
2995      6D43      3E 64      MVI A,TIMOUT      ;SET UP TIME-OUT
2996      6045      32 79 91      STA XTIMER
2997      6D48      HPW130 EQU $
2998      6D48      3A 40 88      LOA IBSTAT      ;FINISHED TRANSFER?
2999      604B      E6 10      ANI EOIBIT
3000      604D      C2 1A 6F      JNZ UNLIST      ;YES, UNLISTEN HP-IB DEVICES
3001      6050      3A 79 91      LOA XTIMER      ;NO, TIME-OUT OCCURRED?
3002      6D53      B7      ORA A
3003      6D54      C2 48 6D      JNZ HPW130      ;NO, CONTINUE CHECKING
3004      6D57      3A 41 88      LOA IBBFAD      ;YES, HAS DMA ADVANCED THE RAM
3005      6D5A      B9      CMP C      ; BUFFER POINTER?
3006      605B      4F      MOV C,A
3007      605C      C2 43 6D      JNZ HPW125      ;YES, PROBABLY OPERATING WITH SLOW DEVICE
3008      6D5F      HPW135 EQU $
3009      605F      3E 40      MVI A,OMAFI      ;NO, DMA HAS STALLED, ERROR
3010      6061      32 5D FE      STA STRT2
3011      6D64      C3 80 6A      JMP DOWN

```

```

=====
ITEM# LOC OBJECT CODE SOURCE STATEMENTS SAMPLE HP-IB DRIVER - 13255-91128 PAGE 74
=====
3013 ;
3014 ; HPIBRD - HP-IB READ DRIVER
3015 ;
3016 ; ENTRY : DATA AREA 2 HAS BEEN SET UP AS FOLLOWS
3017 ;
3018 ; IBADR2 = HP-IB ADDRESS OF DEVICE
3019 ; SECNDY = SECONDARY ADDRESS
3020 ; BFADR2 = BUFFER PTR FOR DATA STORAGE
3021 ; BFLN2 = EXPECTED LENGTH (0=>256)
3022 ; FLAGS2 = ENABLE APPROPRIATE MODES
3023 ;
3024 ; EXIT : NC => NO ERROR OCCURRED
3025 ; A,B,D,E,H,L DESTROYED
3026 ; STRT2 = 0
3027 ; BFLN2 = ACTUAL AMOUNT OF DATA RECEIVED
3028 ;
3029 ; C => ERROR OCCURRED
3030 ; A,B,D,E,H,L DESTROYED
3031 ; STRT2 = ERROR CODE
3032 ;
3033 6D67 HPIBRD EQU $
3034 6D67 CD E8 6E CALL CNTLR ;CONTROLLER-IN-CHARGE?
3035 6D6A DA C1 6D JC HPR040 ;NO,
3036 6D6D D4 1A 6F CNC UNLIST ;UNLISTEN ALL DEVICES
3037 6D70 D4 3D 6F CNC TALKER ;YES, SET DEVICE TO TALK
3038 6D73 D4 2B 6F CNC SECOND ;THEN SEND SECONDARY
3039 6D76 D4 1F 6F CNC TERMLS ; THEN SET TERMINAL TO LISTEN
3040 6D79 D4 C9 6E CNC PHICNT ; AND SET PHI FOR EXPECTED DATA COUNT
3041 6D7C D8 RC ;IF SOMETHING WENT WRONG, RETURN
3042 ;
3043 6D7D 2A 6F 91 LHL D BFADR2 ;GET DATA BUFFER ADDRESS
3044 6D80 1E 00 MVI E,0 ;SET UP BYTE COUNTER
3045 6D82 3A 6D 91 LDA FLAGS2
3046 6D85 E6 80 ANI DMA
3047 6D87 C2 EB 6D JNZ HPR100
3048 6D8A HPR005 EQU $
3049 6D8A CD A6 6E CALL DATAIN ;GET DATA BYTE
3050 6D8D D8 RC
3051 6D8E 70 MOV M,B
3052 6D8F 23 INX H
3053 6D90 1C INR E ;INCREMENT BUFFER POINTER
3054 6D91 CA A3 6D JZ HPR007 ;INCREMENT BYTE COUNT
3055 6D94 57 MOV D,A ;> 256, END XFER
3056 6D95 3A 6D 91 LDA FLAGS2 ;SAVE FLAGS DESCRIBING DATA BYTE
3057 6D98 E6 01 ANI LFDET ;TERMINATE XFER ON 'LF'?
3058 6D9A CA A9 6D JZ HPR010 ;NO
3059 6D9D 78 MOV A,B ;YES, GET DATA BYTE
3060 6D9E FE 0A CPI LF ;IS IT LF?
3061 6DA0 C2 A9 6D JNZ HPR010 ;NO
3062 6DA3 HPR007 EQU $
3063 6DA3 CD F8 6E CALL INITPH ;YES, FLUSH OUTPUT FIFO OF PHI
3064 6DA6 C3 B6 6D JMP HPR020
3065 ;
3066 6DA9 HPR010 EQU $
3067 6DA9 7A MOV A,D ;NO
3068 6DAA E6 03 ANI D0+D1 ;DATA BYTE?
3069 6DAC FE 00 CPI DATA

```

ITEM	LOC	OBJECT CODE	SOURCE STATEMENTS	SAMPLE HP-IB DRIVER - 13255-91128	PAGE 75
3070	6DAE	CA 8A 6D	JZ HPR005	;YES, CONTINUE	
3071	6DB1	FE 01	CPI SECADR	;SECONDARY ADDRESS?	
3072	6DB3	CA 8A 6D	JZ HPR005	;YES, CONTINUE FOR NOW *****	
3073	6DB6		HPR020 EQU \$		
3074	6DB6	7B	MOV A,E		
3075	6DB7	32 6E 91	STA BLEN2	;UPDATE LENGTH OF DATA XFER	
3076	6DBA	CD 43 6F	CALL TERMTK	;RETURN TALK FUNCTION TO TERMINAL	
3077	6DBD	D4 1A 6F	CNC UNLIST	;UNLISTEN HP-IB DEVICES	
3078	6DC0	C9	RET		



ITEM	LOC	OBJECT CODE	SOURCE STATEMENTS	SAMPLE HP-IB DRIVER - 13255-91128	PAGE 77
3107			;		
3108			; DMA INPUT REQUESTED		
3109			;		
3110	6DEB		HPR100 EQU \$		
3111	6DEB	3A 73 91	LDA CNTLWD ;RESET RAM BUFFER POINTER		
3112	6DEE	F6 10	ORI RSTBUF		
3113	6DF0	32 40 88	STA IBCNTL		
3114	6DF3	3A 04 88	LDA PHIRG4 ;SET UP DMA SENSE FROM PHI		
3115	6DF6	E6 FD	ANI ONES-DMASEL		
3116	6DF8	32 04 88	STA PHIRG4		
3117	6DFB	0E 00	MVI C,0		
3118	6DFD	3A 73 91	LDA CNTLWD ;START DMA INPUT OPERATION		
3119	6E00	F6 08	ORI PHI2BF		
3120	6E02	32 40 88	STA IBCNTL		
3121	6E05		HPR105 EQU \$		
3122	6E05	3E 64	MVI A,TIMOUT ;SET UP TIME OUT COUNTER		
3123	6E07	32 79 91	STA XTIMER		
3124	6E0A		HPR110 EQU \$		
3125	6E0A	3A 40 88	LDA IBSTAT ;INPUT DATA UNTIL EOI OR 256 BYTES		
3126	6E0D	E6 38	ANI EOI BIT+BUFFUL+LSTBYT		
3127	6E0F	C2 24 6E	JNZ HPR120		
3128	6E12	3A 79 91	LDA XTIMER ;TIME OUT OCCURRED?		
3129	6E15	B7	ORA A		
3130	6E16	C2 0A 6E	JNZ HPR110 ;NO, CONTINUE CHECKING FOR END OF XFER		
3131	6E19	3A 41 88	LDA IBBFAD ;YES, RAM BUFFER POINTER ADVANCED?		
3132	6E1C	B9	CMP C		
3133	6E1D	4F	MOV C,A		
3134	6E1E	C2 05 6E	JNZ HPR105 ;YES, CONTINUE TRANSFER		
3135	6E21	C3 5F 6D	JMP HPW135		
3136			;		
3137	6E24		HPR120 EQU \$		
3138	6E24	3A 73 91	LDA CNTLWD ;RESET RAM BUFFER POINTER		
3139	6E27	F6 10	ORI RSTBUF		
3140	6E29	32 40 88	STA IBCNTL		
3141	6E2C		HPR125 EQU \$		
3142	6E2C	3A 20 88	LDA IBBFRD ;READ DATA FROM RAM FIFO		
3143	6E2F	77	MOV M,A		
3144	6E30	47	MOV B,A		
3145	6E31	3A 40 88	LDA IBSTAT ;READ TYPE OF DATA BYTE		
3146	6E34	23	INX H ;MOVE DATA TO I/O BUFFER		
3147	6E35	1C	INR E		
3148	6E36	CA 48 6E	JZ HPR130		
3149	6E39	57	MOV D,A		
3150	6E3A	3A 6D 91	LDA FLAGS2 ;STOP XFER ON LF?		
3151	6E3D	E6 01	ANI LFDET		
3152	6E3F	CA 4E 6E	JZ HPR140 ;NO		
3153	6E42	78	MOV A,B ;YES, CHECK FOR LF CHAR		
3154	6E43	FE 0A	CPI LF		
3155	6E45	C2 2C 6E	JNZ HPR125 ;NOT LF, CONTINUE XFER OF DATA		
3156	6E48		HPR130 EQU \$		
3157	6E48	CD FB 6E	CALL INITPH ;IT'S END OF XFER, CLEAR PHI FIFO'S		
3158	6E4B	C3 5B 6E	JMP HPR150 ; IN CASE SOMETHING IS STILL LEFT		
3159			;		
3160	6E4E		HPR140 EQU \$		
3161	6E4E	7A	MOV A,D ;PURE DATA BYTE?		
3162	6E4F	E6 03	ANI D0+D1		
3163	6E51	FE 00	CPI DATA		

```

=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                                SAMPLE HP-IB DRIVER - 13255-91128      PAGE  78
=====
3164      6E53      CA 2C 6E      JZ   HPR125      ;YES, CONTINUE XFER OF DATA
3165      6E56      FE 01      CPI   SECADR     ;SECONDARY ADDRESS?
3166      6E58      CA 24 6E      JZ   HPR120      ;YES, STILL CONTINUE XFER
3167      6E5B                      HPR150 EQU $
3168      6E5B      7B                      MOV  A,E         ;IT'S AN END OF XFER BYTE
3169      6E5C      32 6E 91      STA  BFLEN2      ;UPDATE DATA LENGTH READ IN
3170      6E5F      CD 43 6F      CALL TERMTK      ;RETURN TALK FUNCTION TO CONTROLLER
3171      6E62      D4 1A 6F      CNC  UNLIST      ;UNLISTEN HP-IB DEVICES
3172      6E65      C9                      RET
=====

```

```

=====
ITEM    LOC    OBJECT CODE  SOURCE STATEMENTS                                SAMPLE HP-IB DRIVER - 13255-91128    PAGE 79
=====
3174          ;
3175          ; DATAOT - OUTPUT DATA BYTE VIA PHI
3176          ; ASSUMES TERMINAL IS CURRENTLY ADDRESSED TO TALK
3177          ;
3178          ; ENTRY : A = DATA BYTE
3179          ;
3180          ; EXIT : NC => NO ERROR
3181          ; A DESTROYED
3182          ; STRT2 = 0
3183          ;
3184          ; C => ERROR OCCURRED
3185          ; A,H,L DESTROYED
3186          ; STRT2 = ERROR CODE
3187          ;
3188    6E66          DATAOT EQU $
3189    6E66    47          MOV B,A
3190    6E67    3E 64          MVI A,TIMOUT ;SET UP TIME-OUT COUNT
3191    6E69    32 79 91          STA XTIMER
3192    6E6C          DOT015 EQU $
3193    6E6C    3A 79 91          LDA XTIMER ;TIME-OUT?
3194    6E6F    B7          ORA A
3195    6E70    CA 82 6E          JZ DOT020 ;YES
3196    6E73    3A 00 88          LDA PHIRG0 ;PHI READY TO ACCEPT DATA?
3197    6E76    E6 08          ANI OTFIFO
3198    6E78    CA 6C 6E          JZ DOT015 ;NO, CONTINUE WAITING
3199    6E7B    78          MOV A,B ;YES, RECALL DATA BYTE
3200    6E7C    32 02 88          STA PHIRG2+DATA2
3201    6E7F    C3 70 6F          JMP OKST
3202          ;
3203    6E82          DOT020 EQU $
3204    6E82    3E 41          MVI A,TIMERR
3205    6E84    32 5D FE          STA STRT2
3206    6E87    C3 80 6A          JMP DOWN

```



```

=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                                SAMPLE HP-IB DRIVER - 13255-91128      PAGE  80
=====
3208      ;
3209      ;   EOIOU - OUTPUT DATA BYTE WITH EOI TRUE
3210      ;           ASSUMES TERMINAL IS CURRENTLY TALKER
3211      ;
3212      ;   ENTRY : A = DATA BYTE
3213      ;
3214      ;   EXIT  : NC => NO ERROR
3215      ;           A DESTROYED
3216      ;           STRT2 = 0
3217      ;
3218      ;           C => ERROR OCCURRED
3219      ;           A,H,L DESTROYED
3220      ;           STRT2 = ERROR CODE
3221      ;
3222      6E8A      EOIOU EQU $
3223      6E8A      47      MOV B,A
3224      6E8B      3E 64    MVI A,TIMOUT ;SET UP TIME-OUT
3225      6E8D      32 79 91 STA XTIMER
3226      6E90      EOIO15 EQU $
3227      6E90      3A 79 91 LDA XTIMER ;TIME-OUT OCCURRED
3228      6E93      B7      ORA A
3229      6E94      CA 82 6E JZ  DOT020 ;YES
3230      6E97      3A 00 88 LDA PHIRG0 ;NO, PHI READY FOR DATA?
3231      6E9A      E6 08    ANI OTFIFO
3232      6E9C      CA 90 6E JZ  EOIO15 ;NO, CONTINUE WAITING
3233      6E9F      78      MOV A,B
3234      6EA0      32 12 88 STA PHIRG2+EOI2
3235      6EA3      C3 70 6F JMP OKST

```

```

=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                                SAMPLE HP-IB DRIVER - 13255-91128      PAGE  81
=====
3237          ;
3238          ; DATAIN = INPUT A BYTE FROM THE PHI
3239          ;
3240          ; ENTRY : DON'T CARE
3241          ;
3242          ; EXIT : NC => NO ERROR
3243          ;          A = DATA TYPE FLAGS
3244          ;          EOI,END OF COUNT,SEC
3245          ;          B = DATA BYTE
3246          ;          STRT2 = 0
3247          ;
3248          ;          C => ERROR OCCURRED
3249          ;          A,H,L DESTROYED
3250          ;          SIRT2 = ERROR CODE
3251          ;
3252      6EA6          DATAIN EQU $
3253      6EA6      3E 64          MVI A,TIMOUT ;SET UP TIME-OUT VALUE
3254      6EA8      32 79 91          STA XTIMER
3255      6EAB          DIN015 EQU $
3256      6EAB      3A 79 91          LDA XTIMER ;TIME-OUT OCCURRED?
3257      6EAE      B7              ORA A
3258      6EAF      CA 82 6E          JZ DOT020 ;YES
3259      6EB2      3A 00 88          LDA PHIRG0 ;NO, PHI HAS DATA?
3260      6EB5      E6 04          ANI INFIFO
3261      6EB7      CA AB 6E          JZ DIN015 ;NO, CONTINUE WAITING
3262      6EBA      3A 02 88          LDA PHIRG2 ;GET DATA BYTE
3263      6EBD      47              MOV B,A
3264      6EBE      3A 40 88          LDA IBSTAT ;GET DATA TYPE FLAGS
3265      6EC1      E6 03          ANI D0+D1
3266      6EC3      F5              PUSH PSW
3267      6EC4      CD 70 6F          CALL OKST
3268      6EC7      F1              POP PSW
3269      6EC8      C9              RET

```

```

=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                                SAMPLE HP-IB DRIVER - 13255-91128      PAGE  82
=====
3271      ;
3272      ; PHICNT - TELL PHI HOW MANY BYTES TO EXPECT
3273      ;          ASSUMES TERMINAL IS CONTROLLER
3274      ;          0 => NO BYTE COUNT LIMIT, WAIT FOR EOI
3275      ;
3276      ; ENTRY : BFLN2 = EXPECTED LENGTH
3277      ;
3278      ; EXIT  : NC => NO ERROR
3279      ;          A DESTROYED
3280      ;          STRT2 = 0
3281      ;
3282      ;          C => ERROR OCCURRED
3283      ;          A,H,L DESTROYED
3284      ;          STRT2 = ERROR CODE
3285      ;
3286      6EC9      PHICNT EQU  $
3287      6EC9      3A 6E 91      LDA  BFLN2      ;GET EXPECTED LENGTH
3288      6ECC      PCT005 EQU  $
3289      6ECC      47              MOV  B,A
3290      6ECD      3E 64          MVI  A,TIMOUT  ;SET UP TIME-OUT
3291      6ECF      32 79 91      STA  XTIMER
3292      6ED2      PCT015 EQU  $
3293      6ED2      3A 79 91      LDA  XTIMER      ;TIME-OUT OCCURRED
3294      6ED5      B7              ORA  A
3295      6ED6      CA 82 6E      JZ    DOT020      ;YES
3296      6ED9      3A 00 88      LDA  PHIRG0      ;NO, PHI ACCEPTS DATA?
3297      6EDC      E6 08          ANI  OTFIFO
3298      6EDE      CA 02 6E      JZ    PCT015      ;NO, CONTINUE WAITING
3299      6EE1      78              MOV  A,B
3300      6EE2      32 1A 88      STA  PHIRG2+REC2
3301      6EE5      C3 70 6F      JMP  OKST

```

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=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                                SAMPLE HP-IB DRIVER - 13255-91128      PAGE  83
=====
3303      ;
3304      ;   CNILR - CHECK FOR CONTROLLER-IN-CHARGE
3305      ;
3306      ;   ENTRY : DON'T CARE
3307      ;
3308      ;   EXIT  : NC => TERMINAL IS CURRENTLY CONTROLLER
3309      ;               A DESTROYED
3310      ;               STRT2 = 0
3311      ;
3312      ;               C => TERMINAL IS NOT CONTROLLER
3313      ;               A,H,L DESTROYED
3314      ;               STRT2 = ERROR CODE
3315      ;
3316      6EE8      CNTLR EQU $
3317      6EE8      3A 03 88      LDA PHIRG3      ;CONTROLLER IN CHARGE?
3318      6EEB      E6 10          ANI CIC
3319      6EED      C2 70 6F      JNZ OKST        ;YES, RETURN OK STATUS
3320      6EF0      CTL010 EQU $
3321      6EF0      3E 42          MVI A,NOCIC     ;NO, RETURN N-OK STATUS
3322      6EF2      32 5D FE      STA STRT2
3323      6EF5      C3 80 6A      JMP DOWN
3324      ;
3325      ;   INITPH - CLEAR OUT ANY REMAINING BYTES IN FIFO'S
3326      ;
3327      ;   ENTRY : DON'T CARE
3328      ;
3329      ;   EXIT  : A DESTROYED
3330      ;
3331      6EF8      INITPH EQU $
3332      6EF8      3A 04 88      LDA PHIRG4
3333      6EFB      F6 01          ORI INITFF      ;CLEAR OUT FIFO OF DATA
3334      6EFD      32 04 88      STA PHIRG4      ; FROM PHI OUT FIFO TO STOP ANY
3335      6F00      IPH010 EQU $      ; FURTHER HP-IB HANDSHAKES
3336      6F00      3A 00 88      LDA PHIRG0      ;CLEAR OUT ANY REMAINING BYTES
3337      6F03      E6 04          ANI INFIFO      ; FROM THE IN FIFO OF PHI
3338      6F05      C8            RZ
3339      6F06      3A 02 88      LDA PHIRG2
3340      6F09      C3 00 6F      JMP IPH010

```

```

=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                                SAMPLE HP-IB DRIVER - 13255-91128      PAGE  84
=====
3342      ;
3343      ;  COMMND - OUTPUT HP-IB UNIVERSAL COMMAND
3344      ;          ASSUMES TERMINAL IS CONTROLLER
3345      ;
3346      ;  ENTRY : A = DATA TO BE OUTPUT
3347      ;
3348      ;  EXIT  : SEE 'TALKER'
3349      ;
3350      6F0C      COMMND EQU $
3351      6F0C      FE 20      CPI MAXADR      ;LARGER THAN MAX VALUE?
3352      6F0E      D2 68 6F      JNC TLK030      ;YES, ERROR
3353      6F11      C3 4C 6F      JMP TLK013      ;TRY TO OUTPUT
3354      ;
3355      ;  LISTEN - OUTPUT LISTEN ADDRESS ONTO HP-IB
3356      ;          ASSUMES TERMINAL IS CURRENTLY CONTROLLER
3357      ;
3358      ;  ENTRY : IBADR2 = HP-IB ADDRESS OF DEVICE TO RECEIVE DATA
3359      ;
3360      ;  EXIT  : SEE 'TALKER'
3361      ;
3362      ;  TERMLS - SET UP TERMINAL AS LISTENER
3363      ;
3364      ;  UNLIST - UNLISTEN HP-IB DEVICES
3365      ;
3366      6F14      LISTEN EQU $
3367      6F14      3A 72 91      LDA IBADR2
3368      6F17      C3 21 6F      JMP LIS010
3369      ;
3370      6F1A      UNLIST EQU $
3371      6F1A      3E 1F      MVI A,UNLSAD
3372      6F1C      C3 21 6F      JMP LIS010
3373      ;
3374      6F1F      TERMLS EQU $
3375      6F1F      3E 1E      MVI A,TERMID
3376      ;
3377      6F21      LIS010 EQU $
3378      6F21      FE 20      CPI MAXADR      ;ADDRESS > 32?
3379      6F23      D2 68 6F      JNC TLK030      ;YES, ERROR
3380      6F26      F6 20      ORI LISBIT
3381      6F28      C3 4C 6F      JMP TLK013

```

```

=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                                SAMPLE HP-IB DRIVER - 13255-91128      PAGE 85
=====
3383                                           ;
3384                                           ; SECOND - OUTPUT A SECONDARY ADDRESS TO HP-IB
3385                                           ; ASSUMES TERMINAL IS CONTROLLER
3386                                           ;
3387                                           ; ENTRY : SECNDY = SECONDARY TO BE OUTPUT
3388                                           ; IF = 200B, THEN NO SECONDARY
3389                                           ;
3390                                           ; EXIT : SEE 'TALKER'
3391                                           ;
3392      6F2B                                           SECOND EQU $
3393      6F2B      3A 71 91      LDA SECNDY
3394      6F2E      FE 80      CPI NOSEC      ;NO SECONDARY?
3395      6F30      CA 70 6F      JZ OKST      ;YES
3396      6F33      FE 20      CPI MAXADR      ;NO, LARGER THAN MAX VALUE?
3397      6F35      D2 68 6F      JNC TLK030      ;YES, ERROR
3398      6F38      F6 60      ORI SECBIT      ;NO, TRY TO OUTPUT
3399      6F3A      C3 4C 6F      JMP TLK013

```

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=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                                SAMPLE HP-IB DRIVER - 13255-91128      PAGE  86
=====
3401      ;
3402      ; TALKER - OUTPUT TALK ADDRESS ONTO HP-IB
3403      ; ASSUMES TERMINAL IS CURRENTLY CONTROLLER
3404      ;
3405      ; ENTRY : IBADR2 = HP-IB ADDRESS OF DEVICE TO TALK
3406      ;
3407      ; EXIT : NC => TALK ADDRESS OUTPUT SUCCESSFULLY
3408      ; A DESTROYED
3409      ; STRT2 = 0
3410      ;
3411      ; C => ERROR OCCURRED
3412      ; A,H,L DESTROYED
3413      ; STRT2 = ERROR CODE
3414      ;
3415      ; TERMTK - ENTRY POINT TO SET UP TERMINAL AS TALKER
3416      ;
3417      ; ENTRY : DON'T CARE
3418      ; EXIT : SAME AS 'TALKER'
3419      ;
3420      ; TLK013 - OUTPUT PHI INTERFACE COMMAND (ATN TRUE)
3421      ;
3422      ; ENTRY : A = DATA BYTE
3423      ; EXIT : SAME AS 'TALKER'
3424      ;
3425      ; TLK020 - SET UP TIME-OUT ERROR RETURN
3426      ;
3427      ; ENTRY : STACK HAS EXTRA LEVEL, WHICH WILL BE POP'ED
3428      ; EXIT : SAME AS 'TALKER'
3429      ;
3430      6F3D      TALKER EQU $
3431      6F3D      3A 72 91      LDA IBADR2
3432      6F40      C3 45 6F      JMP TLK010
3433      ;
3434      6F43      TERMTK EQU $
3435      6F43      3E 1E      MVI A,TERMTD ;SET UP TERMINAL ADDRESS
3436      ;
3437      6F45      TLK010 EQU $
3438      6F45      FE 20      CPI MAXADR ;ADDRESS > 32 ?
3439      6F47      D2 68 6F      JNC TLK030 ;YES, ERROR
3440      6F4A      F6 40      ORI TLKBIT ;SET TALK ADDRESS
3441      6F4C      TLK013 EQU $
3442      6F4C      47      MOV B,A ;SAVE VALUE
3443      6F4D      3E 64      MVI A,TIMOUT ;SET UP TIME-OUT VALUE
3444      6F4F      32 79 91      STA XTIMER ; FOR 1 SECOND
3445      6F52      TLK015 EQU $
3446      6F52      3A 79 91      LDA XTIMER
3447      6F55      B7      ORA A ;TIME-OUT OCCURRED?
3448      6F56      CA 82 6E      JZ DOT020 ;YES
3449      6F59      3A 00 88      LDA PHIRGO ;PHI ACCEPT A BYTE?
3450      6F5C      E6 08      ANI UTFIFO
3451      6F5E      CA 52 6F      JZ TLK015 ;NO, CONTINUE WAITING
3452      6F61      78      MOV A,B ;RECALL DATA BYTE
3453      6F62      32 0A 88      STA PHIRG2+IFCOM2 ;OUTPUT
3454      6F65      C3 70 6F      JMP OKST
3455      ;
3456      6F68      TLK030 EQU $ ;RETURN BAD PRESS ERROR CODE
3457      6F68      3E 43      MVI A,BADADR
=====

```

ITEM	LOC	OBJECT CODE	SOURCE STATEMENTS	SAMPLE HP-IB DRIVER - 13255-91128	PAGE 87
3458	6F6A	32 5D FE	STA SIRT2		
3459	6F6D	C3 80 6A	JMP DOWN		



ITEM	LOC	OBJECT CODE	SOURCE STATEMENTS	SAMPLE HP-IB DRIVER - 13255-91126	PAGE 88
3461			;		
3462			; OKST - SET UP OK STATUS RETURN		
3463			;		
3464	6F70		OKST EQU \$		
3465	6F70	AF	XRA A		
3466	6F71	32 5D FE	STA STRT2		
3467	6F74	3E 53	MVI A,S		
3468	6F76	32 4F FF	STA IOCERR		
3469	6F79	C9	RET		

```

=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                                SAMPLE HP-IB DRIVER - 13255-91128      PAGE  89
=====
3471          ;
3472          ; * * * * *
3473          ;
3474          ;      GETPTR - GET POINTER TO FIRST BYTE OF I/O
3475          ;      BUFFER
3476          ;
3477          ;      ENTRY: D,E -> BUFFER STATUS
3478          ;
3479          ;      EXIT : H,L -> FIRST BYTE
3480          ;      A DESTROYED
3481          ;
3482          ;
3483      6F7A          GETPTR EQU $
3484      6F7A      7B      MOV  A,E          ;GET LOW BYTE OF STATUS PTR
3485      6F7B      FE 3A      CPI  B1STAT*256/256 ;COMPARE WITH LOW
3486          ;          ; BYTE OF BUF1 STATUS
3487      6F7D      21 00 FC      LXI  H,IOBUF1
3488      6F80      C8          RZ          ;RETURN IOBUF1 IF SAME
3489      6F81      21 00 FD      LXI  H,IOBUF2
3490      6F84      C9          RET          ;ELSE RETURN IOBUF2

```

```

=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS                SAMPLE HP-IB DRIVER - 13255-91128      PAGE  90
=====
3492      ;
3493      ; * * * * *
3494      ;
3495      ;      RETSCN - SEE IF USER HIT "RETURN"
3496      ;
3497      ;      ENTRY:  DON'T CARE
3498      ;
3499      ;      EXIT :   NC => NO CR
3500      ;              C => CR
3501      ;              IOCERR = U
3502      ;              A,B,C,H,L DESTROYED
3503      ;
3504      ;
3505      6F85      RETSCN EQU  $
3506      6F85      D5      PUSH D
3507      6F86      CD 05 48  CALL ZGETKY      ;ANY NEW KEYS HIT?
3508      6F89      D1      POP  D
3509      6F8A      CA 8F 6F  JZ   RET100      ;YES - LOOK AT IT
3510      6F8D      B7      ORA  A      ;NO - RETURN
3511      6F8E      C9      RET
3512      ;
3513      ;      KEY HIT - IS IT RETURN?
3514      ;
3515      6F8F      RET100 EQU  $
3516      6F8F      FE 0D      CPI 150      ;CHECK FOR ASCII CR
3517      6F91      C2 85 6F  JNZ RETSCN      ;NOT CR - CHECK FOR MORE KEYS
3518      6F94      3E 55      MVI A,U      ;RETURN HIT - SET IOCERR = U
3519      6F96      32 4F FF  STA IOCERR
3520      6F99      37      STC
3521      6F9A      C9      RET

```

```
=====
ITEM      LOC      OBJECT CODE  SOURCE STATEMENTS      SAMPLE HP-IB DRIVER - 13255-91128      PAGE  91
=====
3523      6F9B                                END
=====
```

0 ERRORS FOUND IN ASSEMBLY CODE.

TOTAL ASSEMBLY TIME 0: 8:59  
TOTAL ELAPSED TIME 0: 9:28

SYMBOL	VALUE	REFERENCED ON
ADDR	001F	554
ADDRST	917A	349, 350, 1053, 1076, 2485, 2558
ADRLIS	9178	351, 352, 1089, 2472, 2619
ADRMASK	001F	598, 1054
ADRTLK	9176	353, 354, 1088, 2536, 2664
ALSTRT	6000	611, 613
ALTIO	0010	328, 2496, 2552
ATNENB	0002	533, 1081, 1210, 1227
B1LEN	FF38	321
B1STAT	FF3A	317, 318, 2543, 3485
B1TYPE	FF39	318, 321
B2LEN	FF35	326
B2P080	6A63	2493, 2480
B2P200	6A6B	2503, 2491
B2STAT	FF37	324, 325, 2547
B2TYPE	FF36	325, 326
BADADR	0043	606, 3457
BASE	9100	342
BASE2	FF00	311
BF2PHI	0004	534, 1788, 1969, 2193, 2992
BF2PTP	6A35	2471, 622
BFADR2	916F	362, 363, 2481, 2555, 2912, 2950, 3043, 3088
BFLN2	916E	363, 364, 2484, 2557, 2570, 2913, 2951, 3075, 3104, 3169, 3287
BUFADR	0041	399, 421, 732, 756, 1697, 1709, 1751, 1908, 1985, 2015
BUFFUL	0020	547, 3126
BUFRD	0020	397, 419, 764, 772, 1730, 1920, 2023, 2032
BUFVRT	0020	398, 420, 1702, 1713, 1767, 1771, 1857, 1952, 1956, 2157, 2161, 2166
CHARIN	6B6E	2688, 1042, 2701, 2711, 2730, 2738, 2743, 2747, 2757
CHECK	6BFA	2764, 2692
CHINT	0082	336, 2700, 2737, 2752, 2756
CHK100	6C8B	2854, 2767
CHR200	6BD3	2741, 2732
CHR210	6BE2	2748, 2745
CHRI00	6B6E	2689
CHRI15	6B7E	2696
CHRI20	6B8A	2702, 2739, 2758
CHRI30	6BA0	2716, 2695
CHRI50	6BB9	2728
CIC	0010	486, 952, 1068, 1539, 2691, 3318
CNTL	0040	408, 1046, 1080, 1211, 1229, 1541, 1688, 1722, 1763, 1773, 1779, 1787, 1852, 1887, 1891, 1916, 1948, 1958, 1964, 1968, 1994, 1998, 2078, 2153, 2170, 2188, 2192, 2232, 2236
CNTLR	6EE8	3316, 2904, 3034
CNTLWD	9173	359, 360, 1082, 1209, 1213, 1226, 1228, 2971, 2984, 2991, 3111, 3118, 3138
COMMND	6F0C	3350, 2780, 2805
COMOUT	6437	1448, 1160
CTL010	6EF0	3320, 2939, 3087
CTL1BL	62F1	1149, 1135
CURCOL	FFC1	287, 2709
CURROW	FFC0	286, 2703
D0	0002	543, 549, 696, 777, 1660, 1736, 1826, 1927, 2037, 3068, 3097, 3162, 3265

SYMBOL	VALUE	REFERENCED ON
D1	0001	542, 549, 550, 696, 777, 1660, 1736, 1826, 1927, 2037, 3068, 3097, 3162, 3265
D125	0055	435, 2419, 2420, 2421, 2422, 2423, 2429, 2430, 2431, 2432, 2433
D252	00AA	436, 2399, 2400, 2401, 2402, 2403, 2409, 2410, 2411, 2412, 2413
DATA	0000	602, 3069, 3098, 3163
DATA2	0000	566, 650, 1566, 1580, 1627, 1702, 1767, 1857, 1874, 1952, 2157, 2166, 2978, 3200
DATAIN	6EA6	3252, 3049, 3091
DATOUT	6E66	3188, 1441, 2735, 2922, 2958
DCL	0014	591
DEVCLR	0001	471
DIN015	6EAB	3255, 3261
DMA	0080	367, 2916, 3046
DMAACT	0040	548, 730, 754, 1783, 1796, 1810, 1900, 1914, 1977, 2007
DMAFL	0040	603, 3009
DMASEL	0002	502, 1776, 1961, 2173, 2988, 3115
DOT015	6E6C	3192, 3198
DOT020	6E82	3203, 3195, 3229, 3258, 3295, 3448
DOWN	6A80	2512, 3011, 3206, 3323, 3459
DSPMSG	0040	335, 2267, 2292
EIGHT	0038	457, 852, 1946, 2373
ELEVEN	003B	460, 864, 2151
ENDBIT	0080	403, 1713, 1771, 1956, 2161, 2983
ENDTBL	0080	447, 2394, 2404, 2414, 2424, 2434, 2445, 2455
ENDTST	693E	2257, 2252
EOI015	6E90	3226, 3232
EOI2	0010	567, 662, 1632, 1713, 1771, 1880, 1956, 2161, 2983, 3234
EOIBIT	0010	401, 727, 751, 1793, 1897, 1974, 2004, 2999, 3126
EOIOUT	6E8A	3222, 1432, 2928, 2964
EOISTT	0010	546
EOITYP	0003	402, 787
EOP	00CE	307, 2299, 2300, 2519
ERR00	69AF	2340, 1574, 1618, 1654, 1700, 1733, 1784, 1901, 1978
ERR01	69B4	2344, 1587, 1637, 1665, 1712, 1740, 1797, 1905, 1982, 2085, 2126, 2197
ERR02	69B9	2348, 1596, 1668, 1744, 1801, 1911, 1988, 2092, 2133, 2204
ERR03	69BE	2352, 1673, 1749, 1807, 1915, 2008
ERR04	69C3	2356, 1675, 1754, 1811, 1923, 2012, 2241
ERR05	69C8	2360, 1532, 1679, 1930, 2018, 2248
ERR06	69CD	2364, 1540, 1830, 1936, 2027
ERR07	69D2	2368, 1833, 1938, 2041
ERR08	69D7	2372, 1838, 2044
ERR09	69DC	2376, 1840, 2049
ERR10	69E1	2380, 1844, 2051
ERRI00	613A	819
ERRI01	613F	823
ERRI02	6144	827
ERRI03	6149	831, 645, 690
ERRI04	614E	835, 667, 700
ERRI05	6153	839, 702
ERRI06	6158	843, 708, 728
ERRI07	615D	847, 710, 731
ERRI08	6162	851, 714, 735

SYMBOL	VALUE	REFERENCED ON
ERRI09	6167	855, 739, 752
ERRI10	616C	859, 755
ERRI11	6171	863, 759
ERRI12	6176	867, 767
ERRI13	617B	871, 781
ERRI14	6180	875, 784
ERRI15	6185	879, 789
ERRI16	618A	883, 791
ERRI17	618F	887, 795
ERRINT	0001	388, 672, 898, 899, 2066, 2067, 2095, 2109, 2110, 2137, 2178, 2179, 2207, 2218, 2219, 2251
ERRMS2	6977	2298, 2287
ERRNO	FE54	392, 2285
ERROR2	6953	2281, 1820, 2099, 2141, 2211, 2255, 2342, 2346, 2350, 2354, 2358, 2362, 2366, 2370, 2374, 2378, 2382
ERROR4	6952	2274, 2335
ERRORI	6191	892, 821, 825, 829, 833, 837, 841, 845, 849, 853, 857, 861, 865, 869, 873, 877, 881, 885
ESC	0018	312, 2750
F	0046	298, 2293, 2515
FCSW	0080	557, 2486, 2559
FIN	0002	389, 672, 673, 898, 899, 2066, 2087, 2109, 2128, 2178, 2199, 2218, 2243
FIVE	0035	454, 840, 1720, 2361
FIVTEN	003F	464, 880
FLAGS2	916D	364, 1084, 2487, 2561, 2915, 2953, 3045, 3056, 3150
FLGSAV	FE5C	382, 383, 805, 2063, 2175, 2215
FLGSV1	FE5B	383, 384, 808, 2064, 2176, 2216
FORTEN	003E	463, 876
FOUR	0034	453, 836, 1526, 1686, 2357
FREEZE	0001	482, 1563, 2507, 2583, 2726, 2947
GET	0008	585
GETCTL	0014	599, 1058
GETPTR	6F7A	3483, 2476, 2554
GTL	0001	583
HALFBR	008A	306
HIBCNT	FE58	385, 386, 646, 654, 698, 2072, 2115
HIBERN	FE57	386, 387, 894, 2070, 2097, 2113, 2139, 2182, 2209, 2222, 2253
HIBSTT	FE56	387, 391, 671, 674, 810, 897, 900, 2065, 2068, 2083, 2086, 2094, 2108, 2111, 2124, 2127, 2136, 2177, 2180, 2195, 2198, 2206, 2217, 2220, 2239, 2242, 2250
HIBVEC	FE59	384, 385, 633, 670, 896, 1098, 2074, 2117, 2184, 2225
HNDS2	0018	570
HPIB	0088	413, 414, 641, 686, 723, 747, 1045, 1208, 1225, 1257, 1267, 1277, 1287, 1298, 1308, 1318, 1328, 1555, 2077, 2120, 2187, 2228, 2307, 2326
HPIBAD	8800	414, 415, 416, 417, 419, 420, 421
HPIBRD	6D67	3033, 2563
HPIBWR	6CA6	2903, 2489
HPR005	6D8A	3048, 3070, 3072
HPR007	6DA3	3062, 3054
HPR010	6DA9	3066, 3058, 3061
HPR020	6DB6	3073, 3064
HPR040	6DC1	3084, 3035



SYMBOL	VALUE	REFERENCED ON
=====	=====	=====
HPR045	6DCE	3090, 3099, 3101
HPR060	6DE4	3102, 3096
HPR100	6DEB	3110, 3047
HPR105	6E05	3121, 3134
HPR110	6E0A	3124, 3130
HPR120	6E24	3137, 3127, 3166
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